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MS-7276 uATX Version: 10

CPU: Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe family processors in LGA775 Package.

System Chipset:

Intel BroadwaterG965/Q965 (North Bridge)
Intel ICH8DO / DH (South Bridge)

On Board Device:

BIOS -- SPI Flash 8M
Azalia Codec -- ALC883
LPC Super I/O -- W83627DHG
LAN -- NINEVEH/EKRON
CLOCK Gen -- ICS 9LPR502 (56pin)
1394 Controller -- VT6307 (2-port)
Hi-USB to PATA Bridge -- JM20335

Main Memory:

Dual-channel DDR-II * 4 (Max 4GB)

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

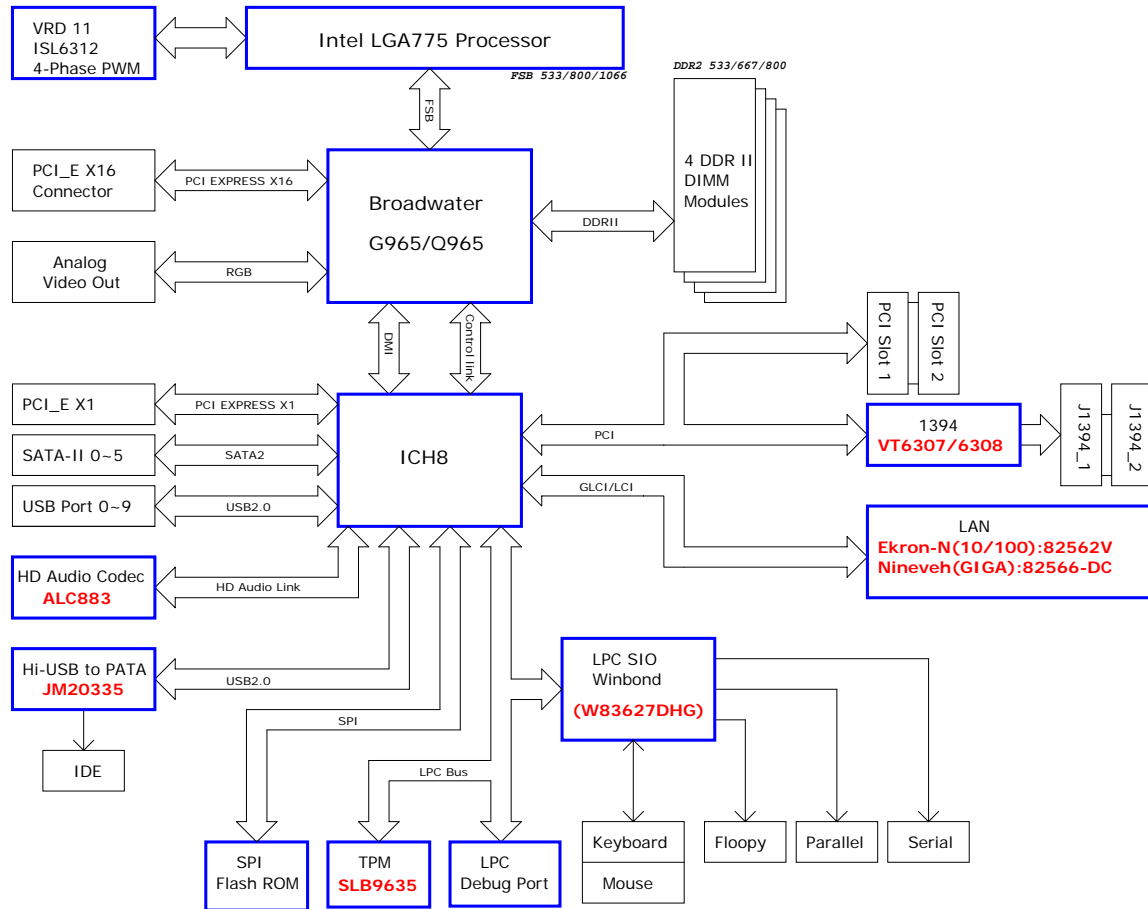
Intersil PWM:

Controller: Intersil ISL6312 (4 Phases)
Driver: Intersil ISL6612

Option	Function	Orcad Configure	BOM
STD	Broadwater/ICH8/W83627DHG/ALC883/82566DM/USB to IDE	cfg-STD	601-7276-A10
OPT:B	Broadwater/ICH8/W83627DHG/ALC883/82562V/USB to IDE	cfg-82562V	601-7276-A20
OPT:C	G965/ICH8DH/W83627DHG/ALC883/82566DC/JM20335	cfg-82566DC	

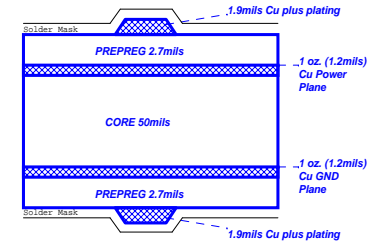
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MS-7276			
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Block Diagram



Board Stack-up

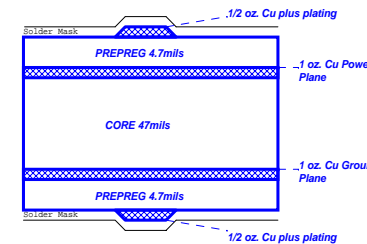
(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15

Board Stack-up

(2116 Prepreg Considerations)



Single End 60ohm Top/Bottom : 5mils
 IEEE1394 - 110ohm Top : 5/7/5
 PCIE, LAN, SATA - 100ohm Top : 5/6/5
 USB2.0 - 90ohm Top : 7.5/7.5/7.5

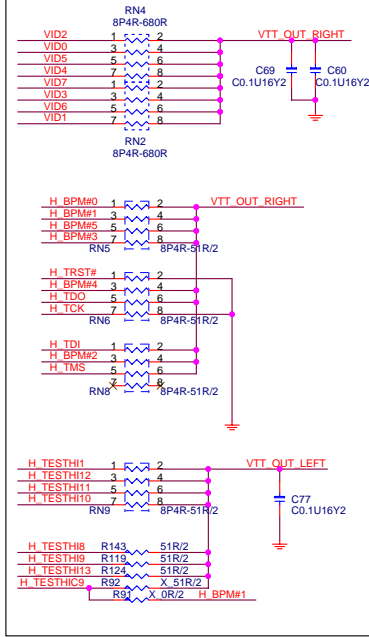
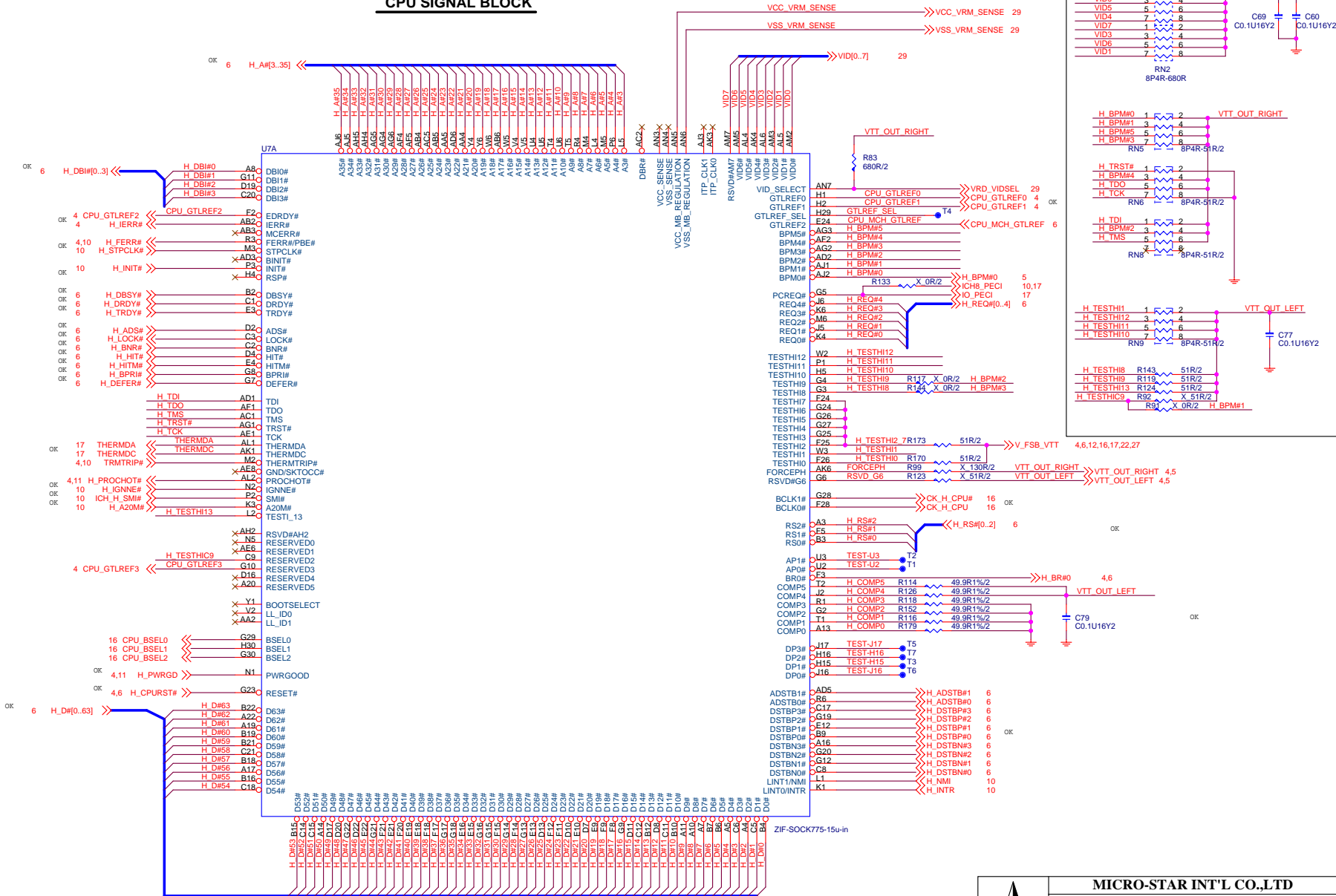


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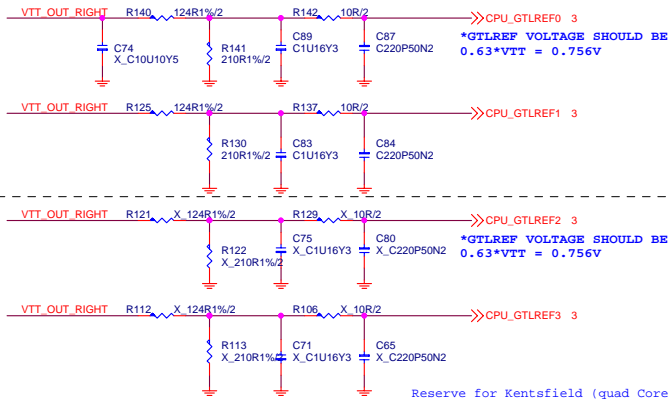
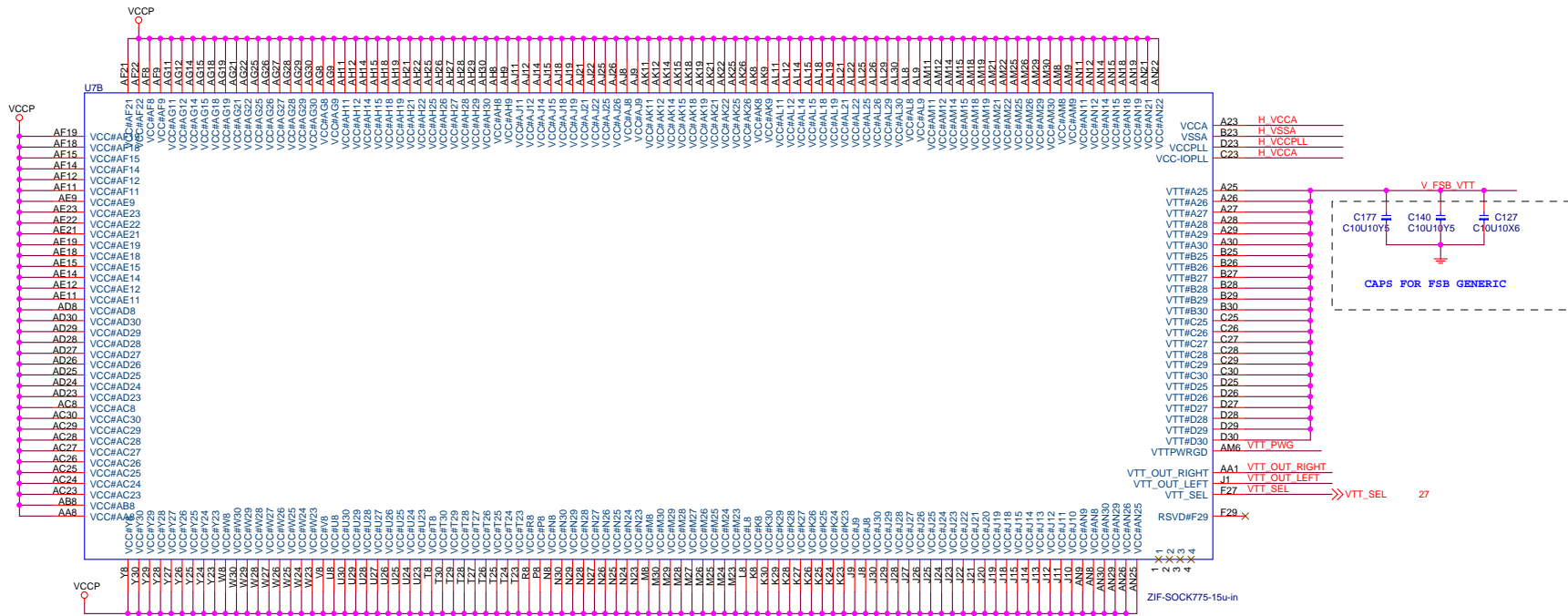
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		BLOCK DIAGRAM	10
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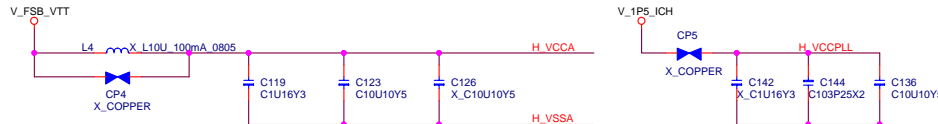
CPU SIGNAL BLOCK



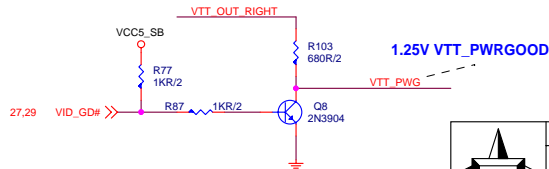
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MS-7276		
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*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS

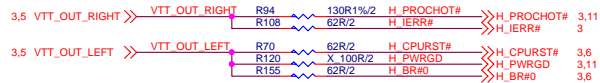


VTT_PWRGOOD

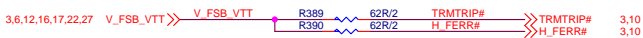


VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

PLACE AT CPU END OF ROUTE



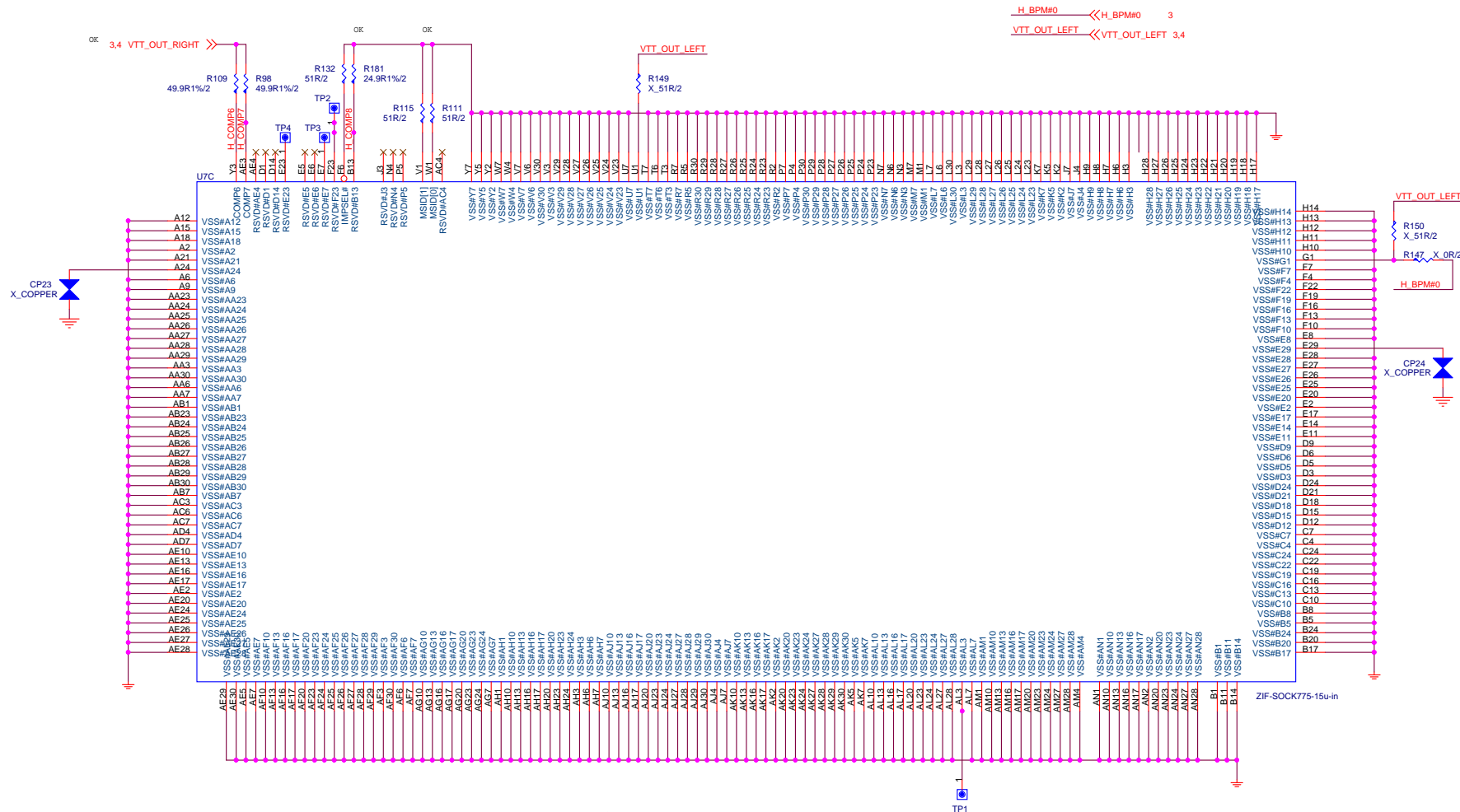
PLACE AT ICH END OF ROUTE



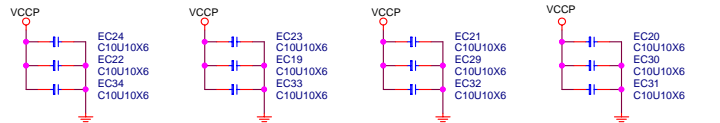
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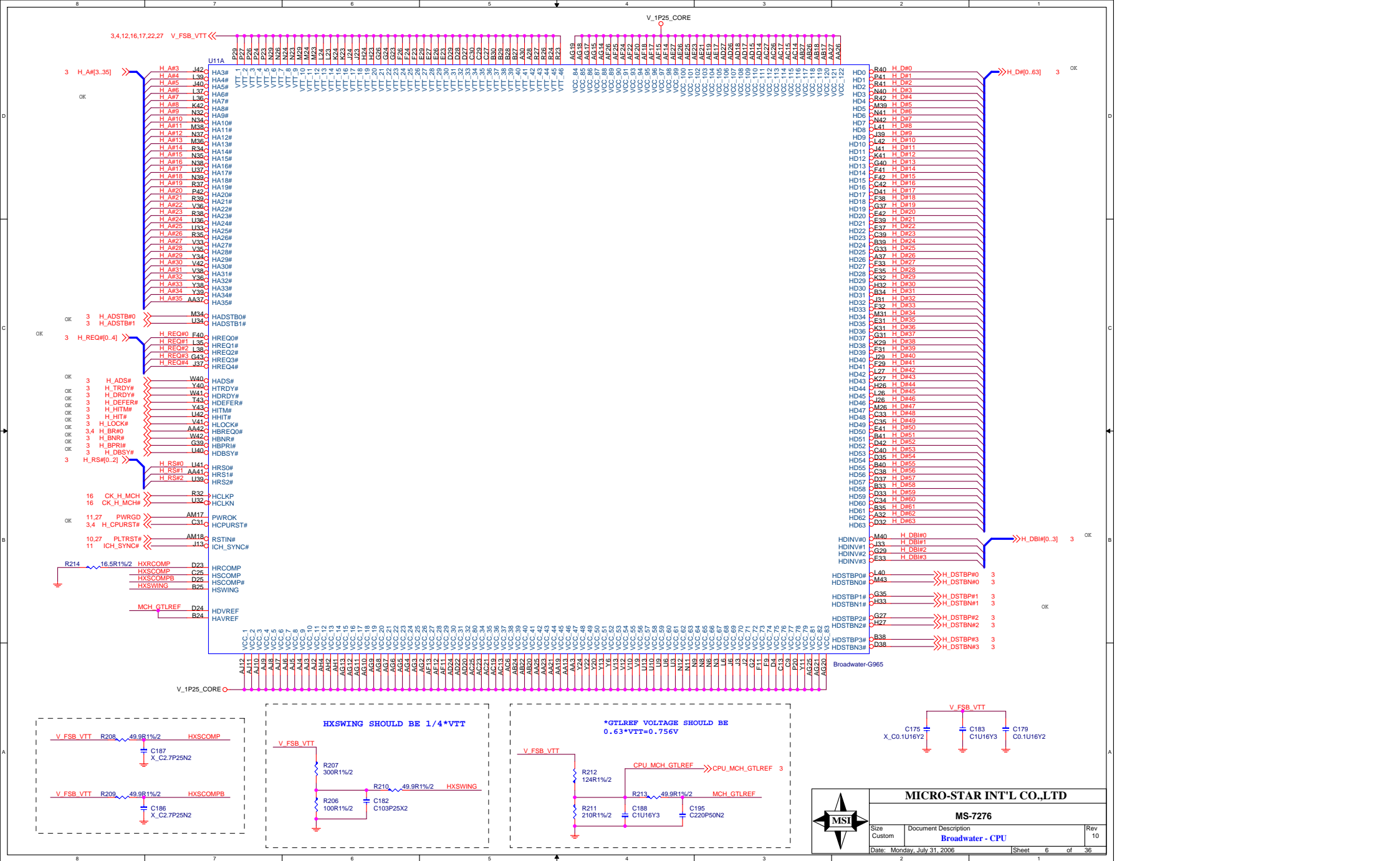


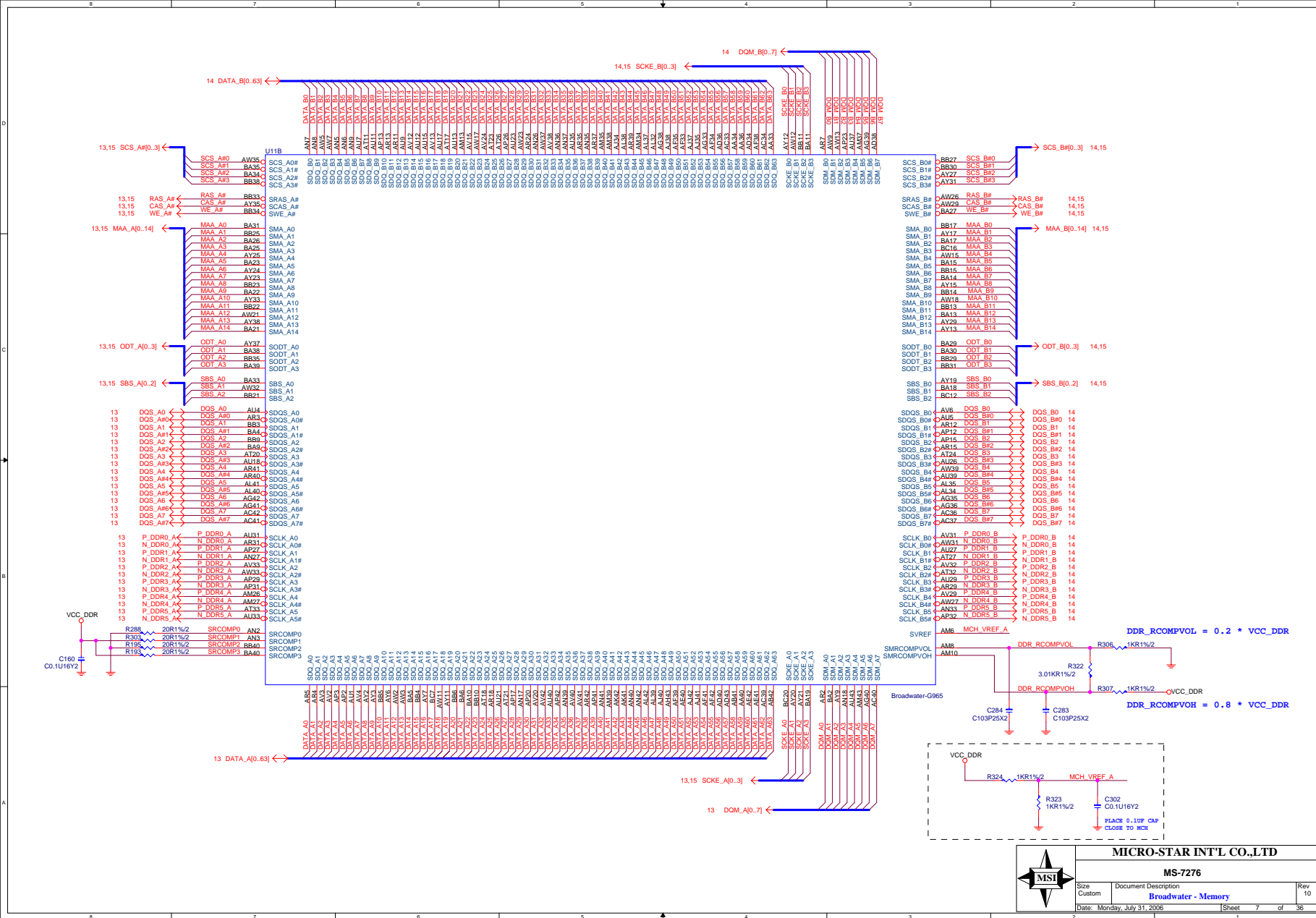
CPU DECOUPLING CAPACITORS

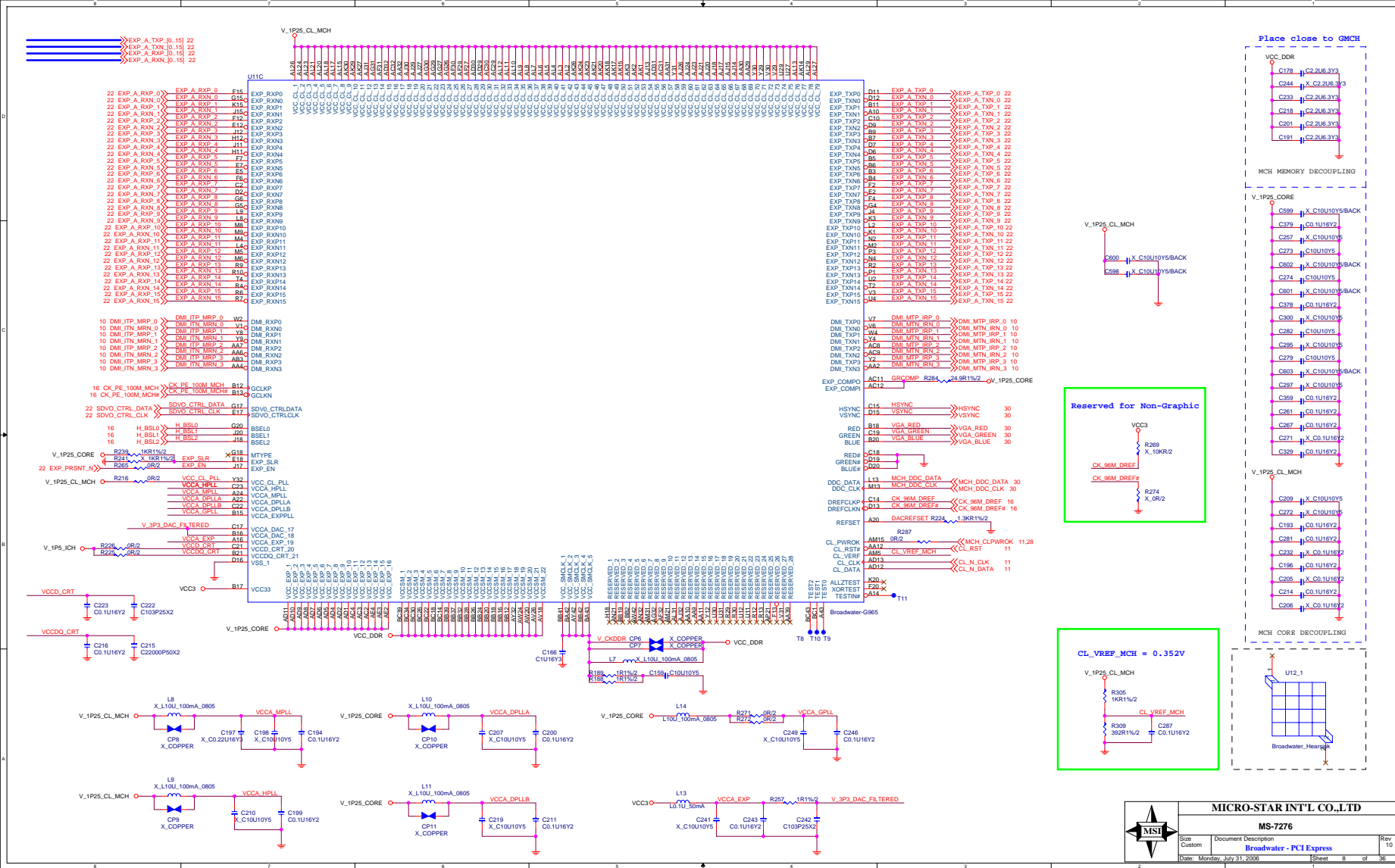


Place these caps within socket cavity

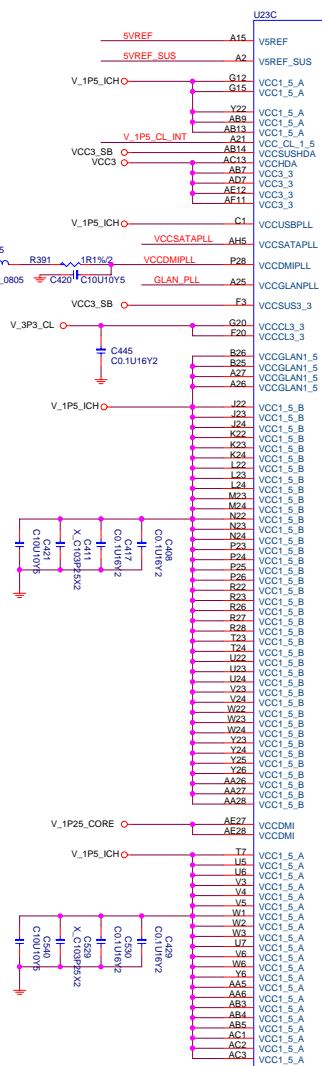
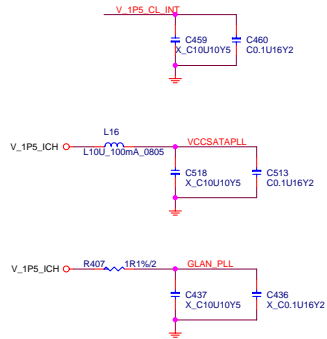
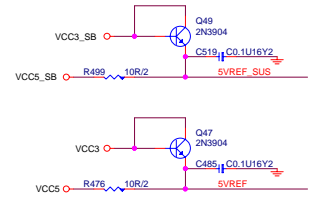
MICRO-STAR INT'L CO.,LTD		
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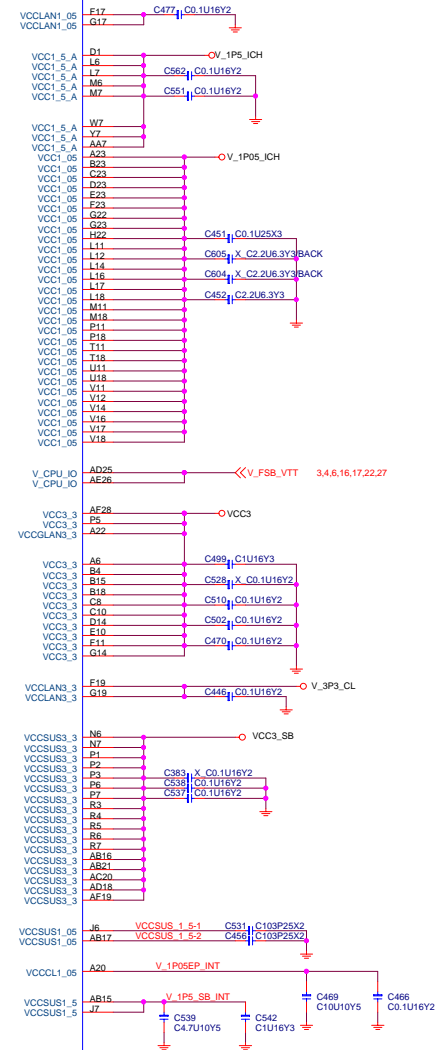
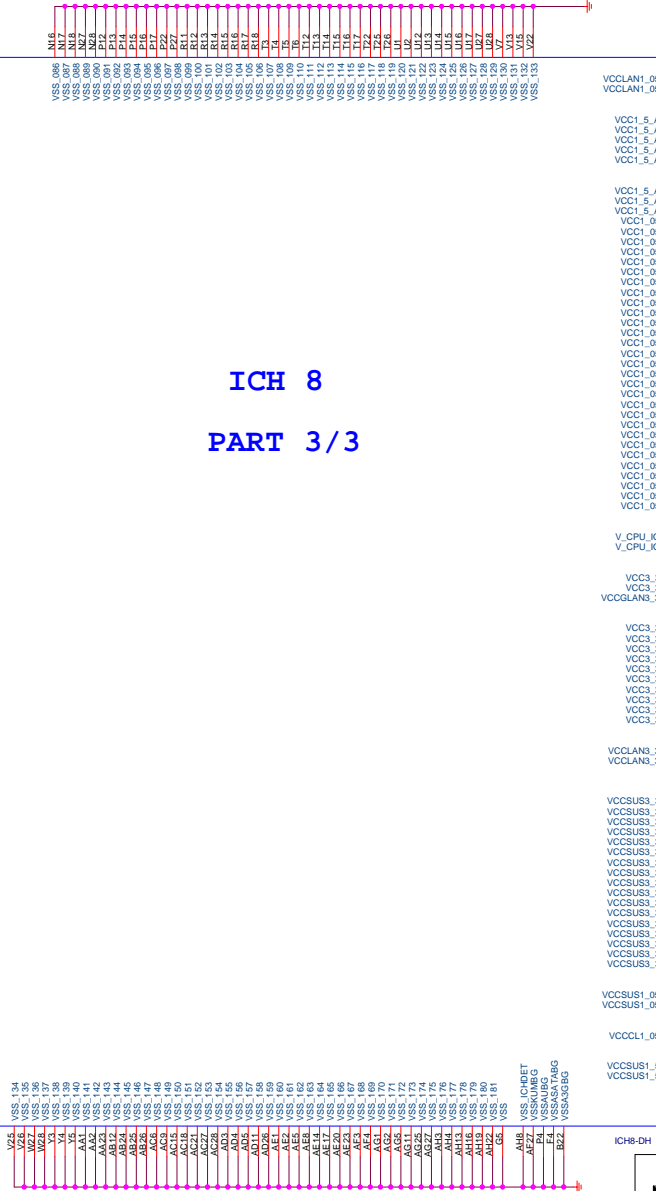




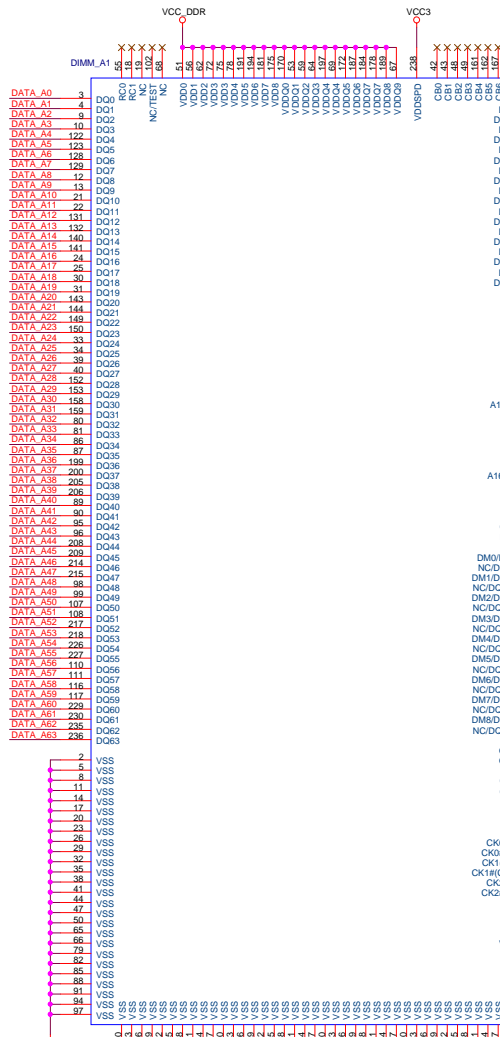
5VREF & 5VREF_SUS Sequencing Circuit



ICH 8
PART 3/3



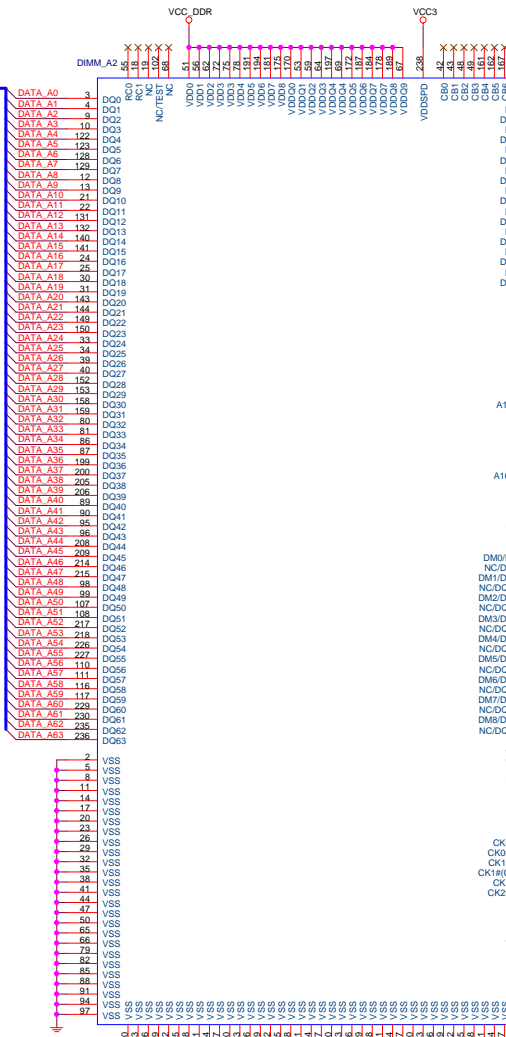
MICRO-STAR INT'L CO.,LTD			
MS-7276			
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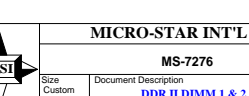
DDRII DIMM_A1



ADDRESS: 000
0xA0



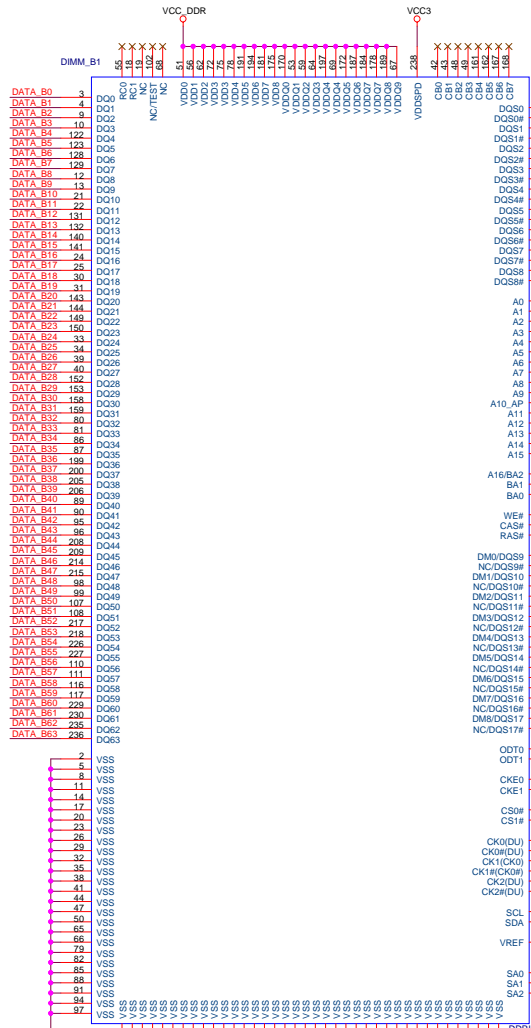
DDRII DIMM_A2



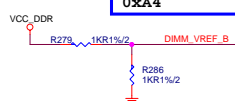
ADDRESS: 001
0xA2



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Custom	DDR II DIMM 1 & 2	10
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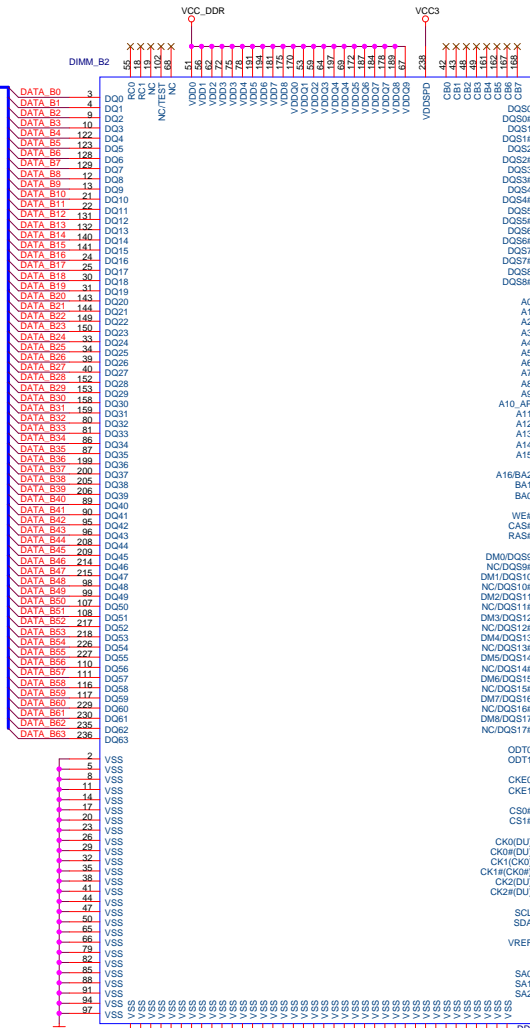


DDR II DIMM_B1



ADDRESS: 010
0xA4

SMBCLK_DDR << SMBCLK_DDR 13
SMBDATA_DDR << SMBDATA_DDR 13



DDR II DIMM_B2

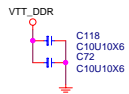
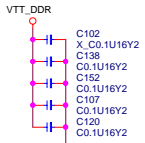
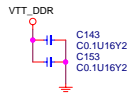


MICRO-STAR INT'L CO.,LTD

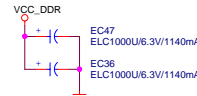
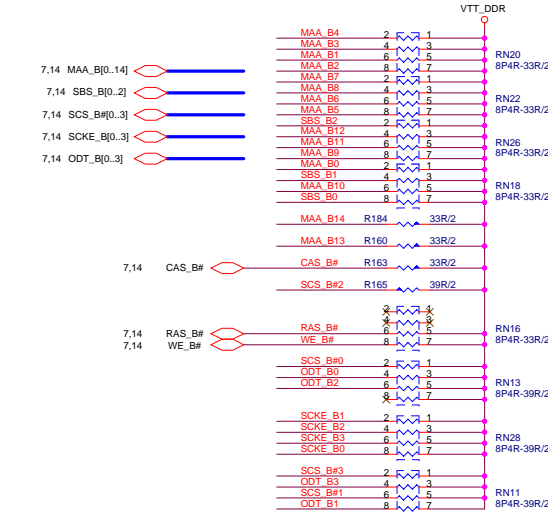
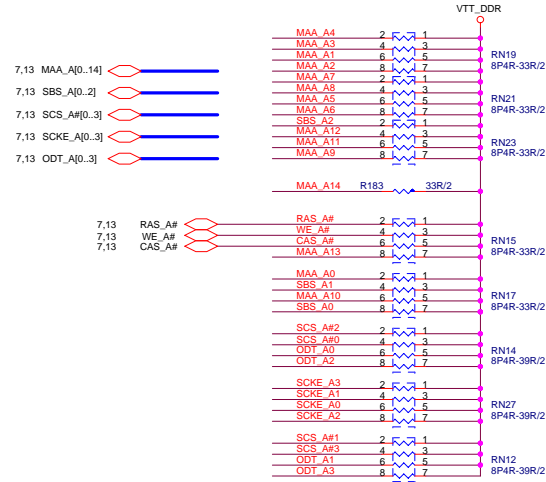
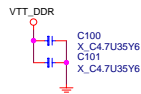
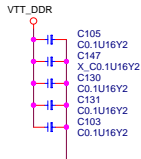
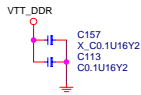
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Custom	DDR II DIMM 3 & 4	10
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CHANNEL A V_{SM_VTT}
DECOUPLING CAPS



CHANNEL B V_{SM_VTT}
DECOUPLING CAPS

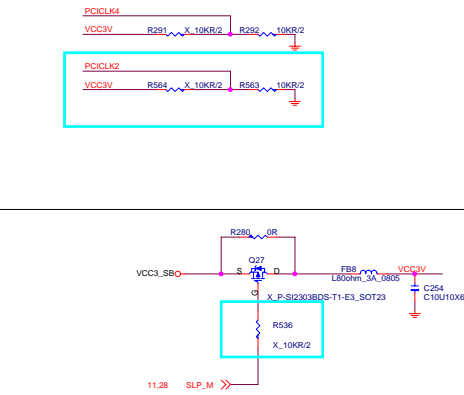
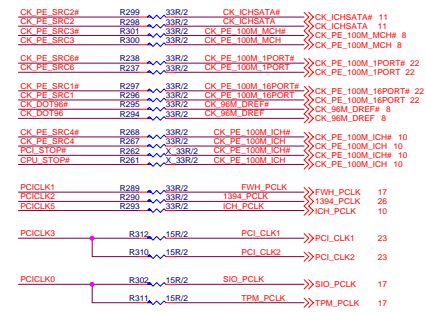
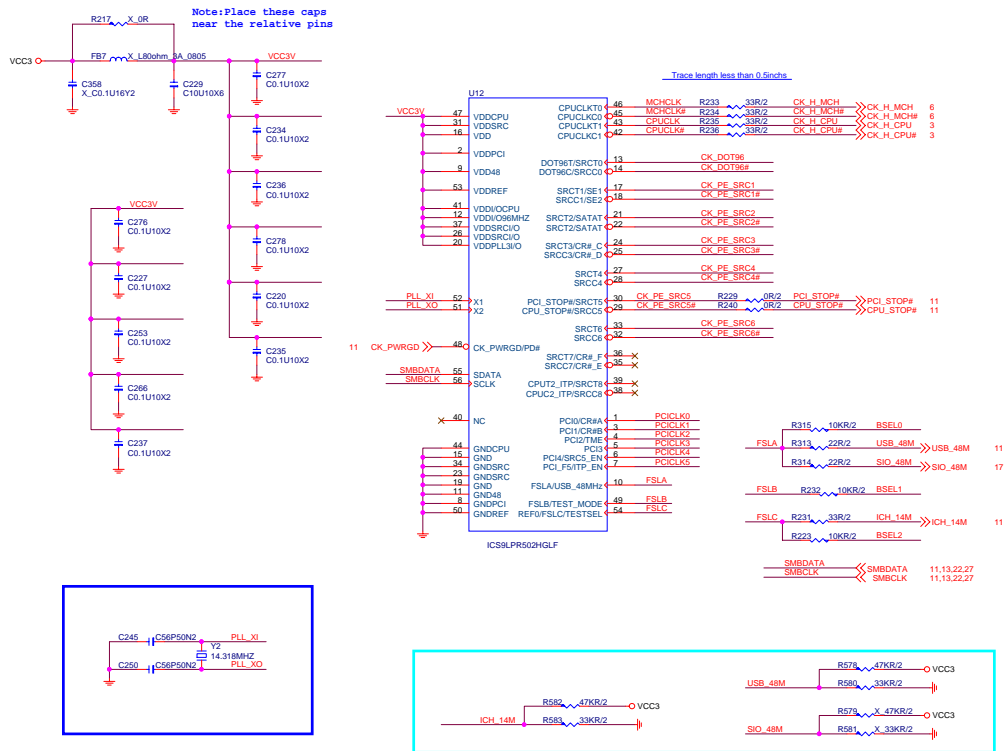


MICRO-STAR INT'L CO.,LTD

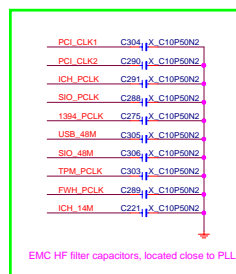
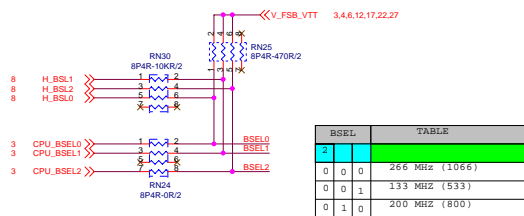
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Clock Generator - ICS9LPR502



BSEL[0..2] Level Shift




MICRO-STAR INT'L CO.,LTD

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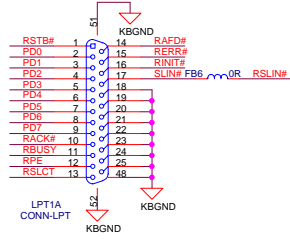
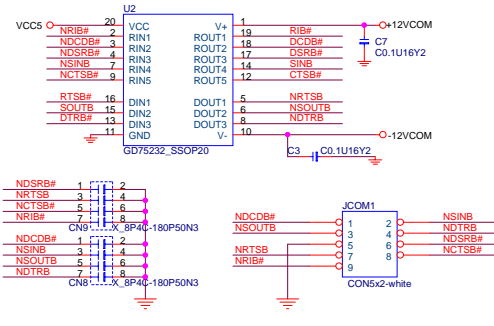
Size Custom	Document Description Clock Gen ICS9LPR502
----------------	---

Date: Monday, July 31, 2006

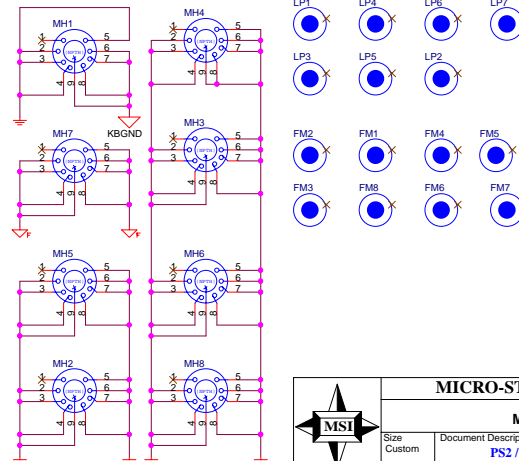
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	MICRO-STAR INT'L CO.,LTD		
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SERIAL PORT 2



Optics Orientation Holes



The schematic diagram shows two connections. The top connection is labeled 'VCC5' and is connected to the top pin of a component labeled 'J1'. The bottom connection is connected to a ground symbol and the bottom pin of a component labeled 'J2'. Both connections are marked with a red 'X'.



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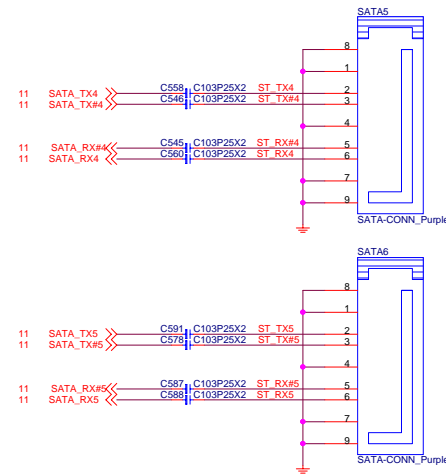
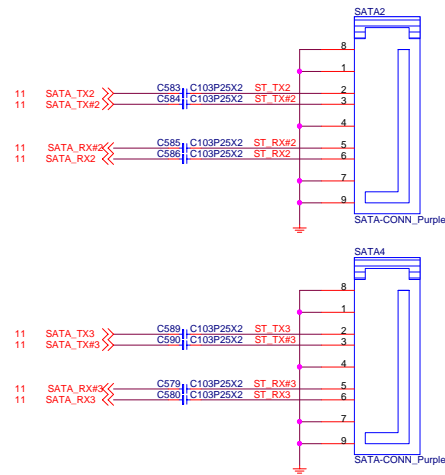
layout時應注意：將KBGND與GND，在第三層用三個50mil的通道相連

SATA CONNECTOR BLOCK

The diagram illustrates the internal wiring of a SATA connector block, showing two connector types: SATA1 and SATA3. Each connector is represented by a blue U-shaped outline with pins numbered 1 through 8. The wiring is as follows:

- SATA1:**
 - Pin 1: Connected to C563, C103P25X2, and ST_TX0.
 - Pin 2: Connected to C564, C103P25X2, and ST_TX#0.
 - Pin 3: Connected to C565, C103P25X2, and ST_RX#0.
 - Pin 4: Connected to C566, C103P25X2, and ST_RX0.
 - Pin 5: Connected to C555, C103P25X2, and ST_RX#0.
 - Pin 6: Connected to C556, C103P25X2, and ST_RX0.
 - Pin 7: Grounded.
 - Pin 8: Grounded.
 - Pin 9: Grounded.
- SATA3:**
 - Pin 1: Connected to C552, C103P25X2, and ST_TX1.
 - Pin 2: Connected to C553, C103P25X2, and ST_TX#1.
 - Pin 3: Connected to C549, C103P25X2, and ST_RX#1.
 - Pin 4: Connected to C550, C103P25X2, and ST_RX1.
 - Pin 5: Connected to C549, C103P25X2, and ST_RX#1.
 - Pin 6: Connected to C550, C103P25X2, and ST_RX1.
 - Pin 7: Grounded.
 - Pin 8: Grounded.
 - Pin 9: Grounded.

The diagram is labeled "SATA-CONN_Purple" at the bottom right.



Close to Pin AD21 of ICH8

Clear CMOS

1 - 2	Normal	★
2 - 3	Clear CMOS	

JBAT1

1
2
3

PHT-3/BLACK

The schematic diagram illustrates the Winbond Protection circuit. It features a +12V supply connected to a diode D15 (1N4148S) and a resistor R194 (4.7K/R/2). The output of D15 is connected to R197 (27K/R/2), which in turn connects to pin 4 of the SYSFAN1 connector. Pin 1 of SYSFAN1 is connected to R196 (10K/R/2), which leads to ground. Pins 2 and 3 of SYSFAN1 are connected to capacitors C164 (4.7uF/10Y5) and C170 (4.7uF/10Y5) respectively, both connected to ground. Pin 1 of SYSFAN1 is also connected to R202 (X 200/R/2), which connects to R203 (X 1K/R/2). The output of R203 is connected to diode D16 (1N4148S). The output of D16 is connected to R201 (0R/R/2), which leads to ASFC_PWM1 (11). Additionally, the output of D16 is connected to R199 (0R/R/2), which leads to SFAN_TACH (11), and to R192 (X 0R/R/2), which leads to SFAN_OUT (17). The circuit is labeled 'Winbond Protection circuit'.

CLEAR CMOS	
1 - 2	Normal ★
2 - 3	Clear CMOS

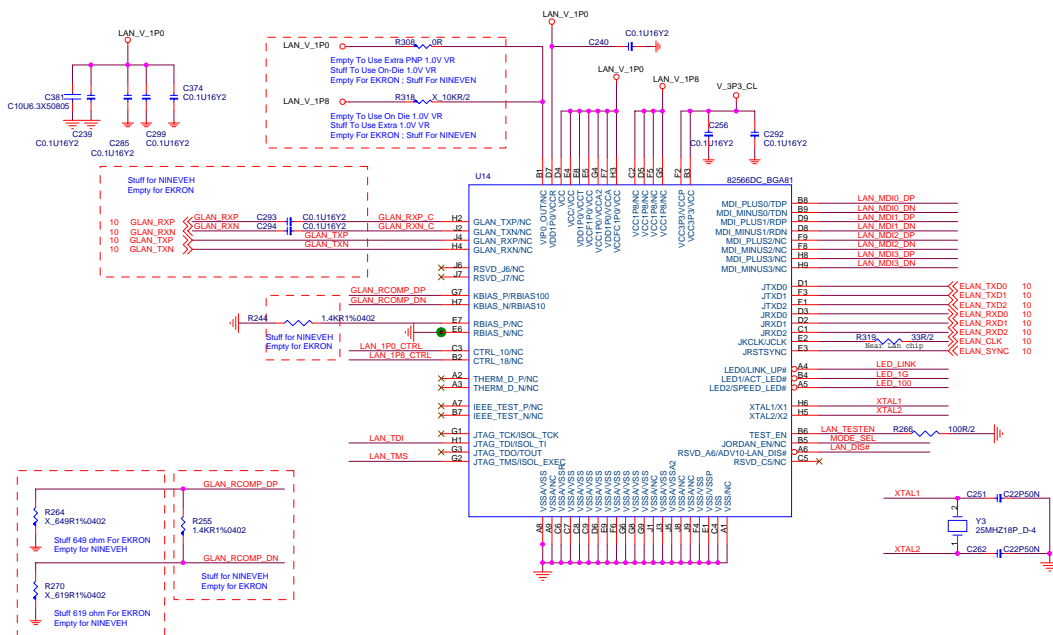


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LAN - NINEVEH/EKRON



Intel® E5560M
 For business desktop PCs.Supports Intel AMT2 or ASF 2.0 alerting,Circuit Breaker,WoL,PXE,Multipoint teaming,RSS,Intel Stable Image Platform Program drivers
 Intel® E5560C
 For consumer desktop PC.Supports Digital Home capabilities,WoL,PXE.
 Intel® E5952V
 Basic 10/100 Ethernet connection.

B0J-825660-1Y1
 FOR MFCP CONSIGN,CHIP LAN,INTEL®E5560M,BGA-8pin,NINEVEY GIGA LAN CHIP(PHY),R0HS COMPLIANCE

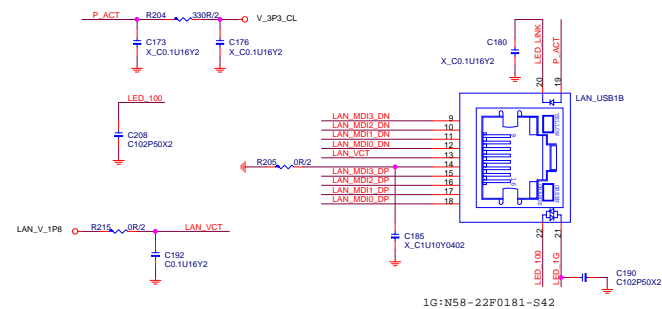
B0J-825661-106
 ,CHIP LAN,INTEL®E5560C,BGA-8pin,NINEVEY GIGA LAN CHIP(PHY),R0HS COMPLIANCE

B0J-825620-106
 CHIP LAN,INTEL®E5952V,BGA-8pin,NINEVEY GIGA LAN CHIP(PHY),R0HS COMPLIANCE




```
Speed LED Type
1000Mbps : Orange
100Mbps  : Green
10Mbps   : LED off
```

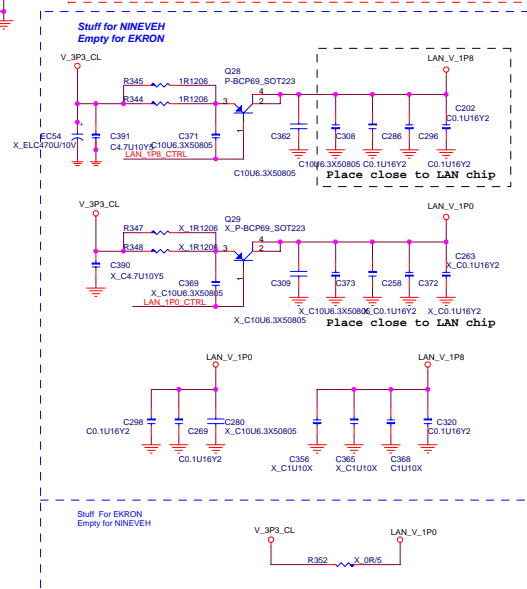
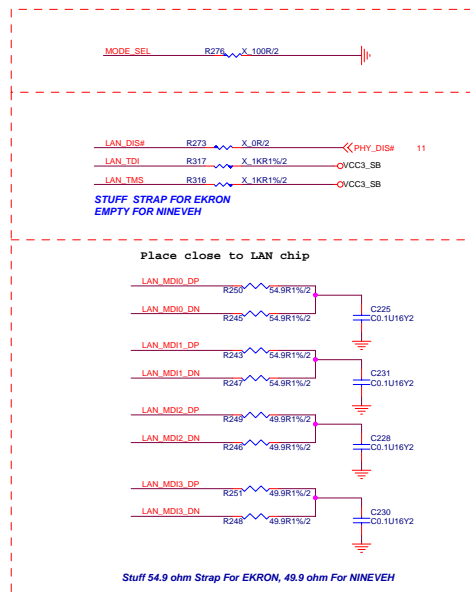
YELLOW : For Active/Link

LAN CONNECTOR



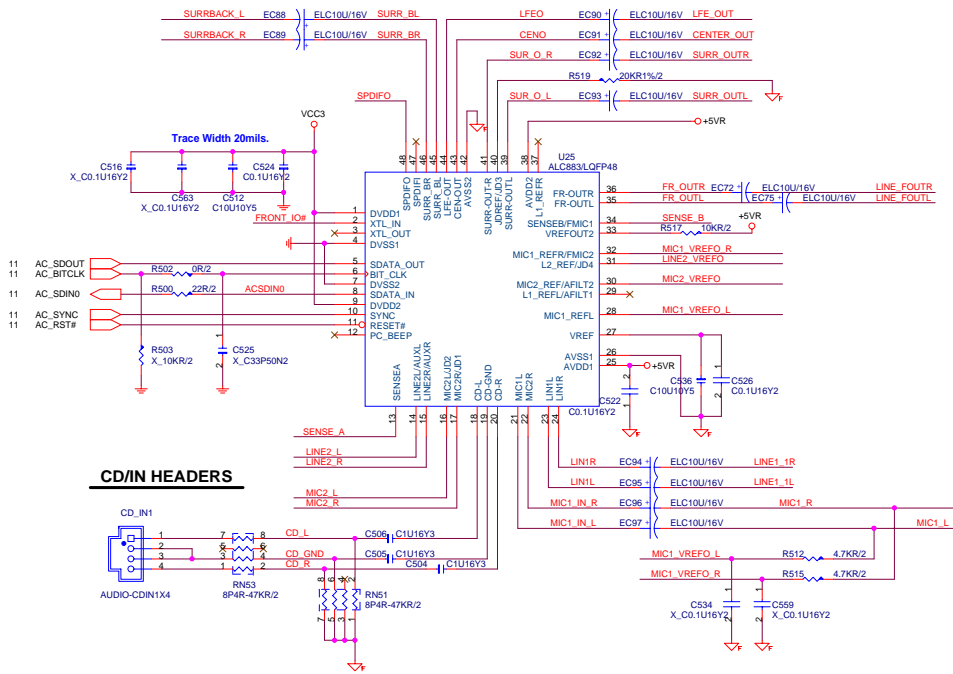
ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN->LOW WOL DIS->HIGH

Giga-Lan		10/100-Lan	
N58-22F0181-642		N58-22F0061-642 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green

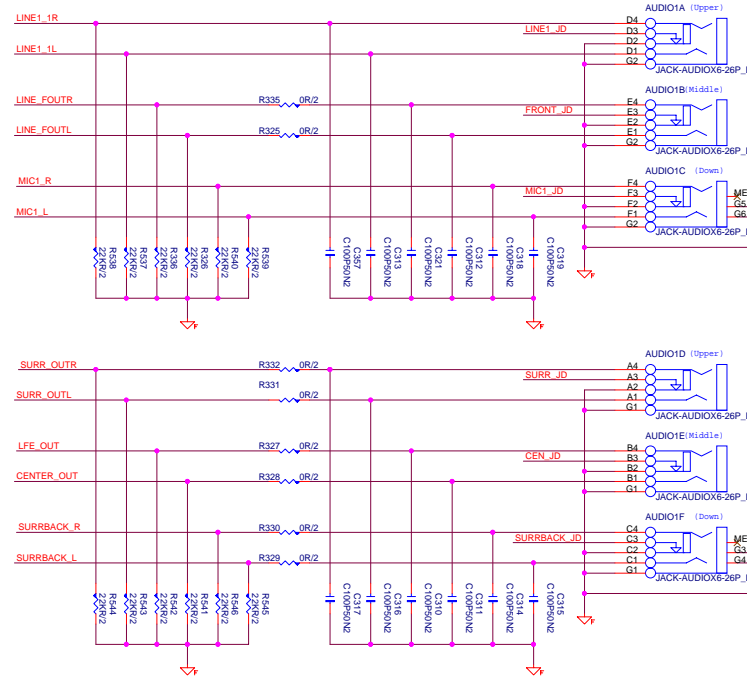


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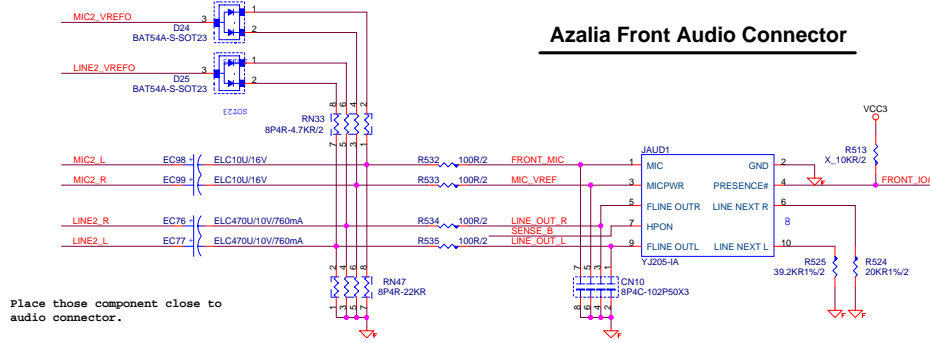
ALC883 CODEC



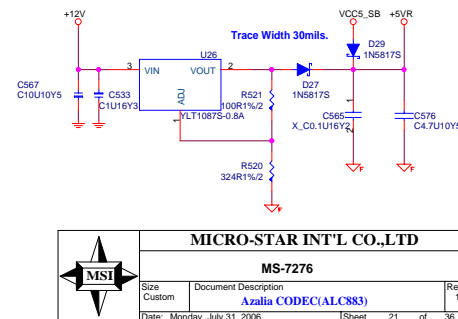
ALC883 JACK



Azalia Front Audio Connector

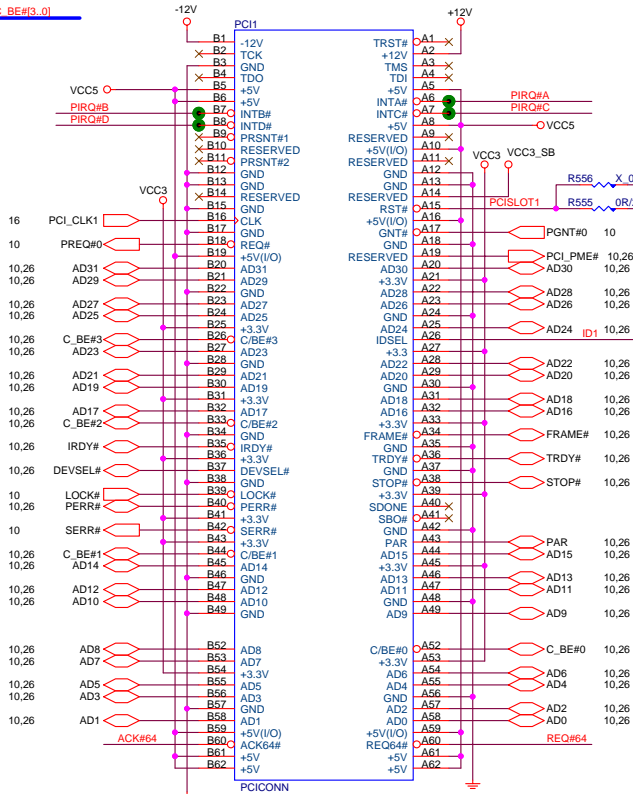


AUDIO CODE REGULATORS



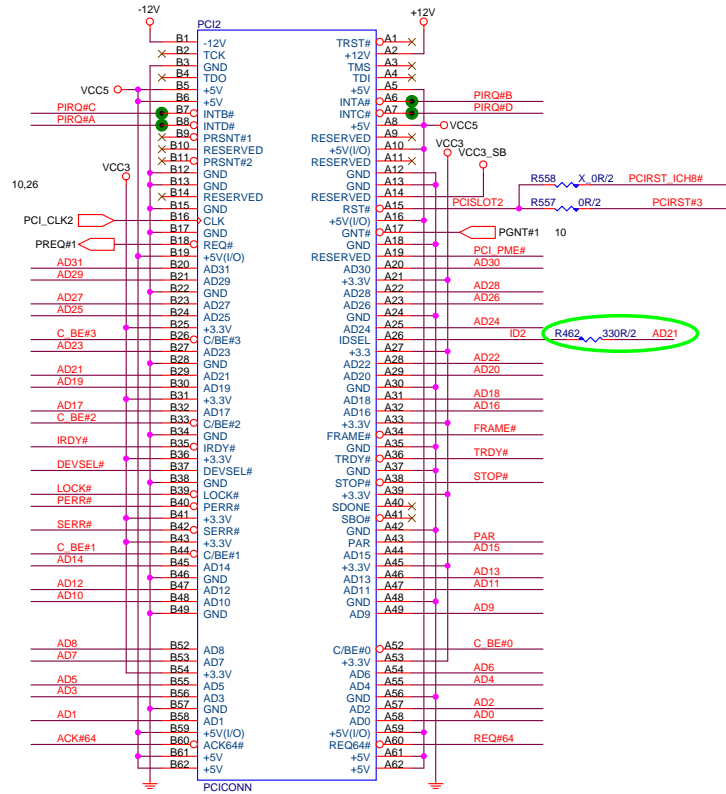
10,26 AD[31..0] << AD[31..0]
10,26 C_BE#[3..0] << C_BE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



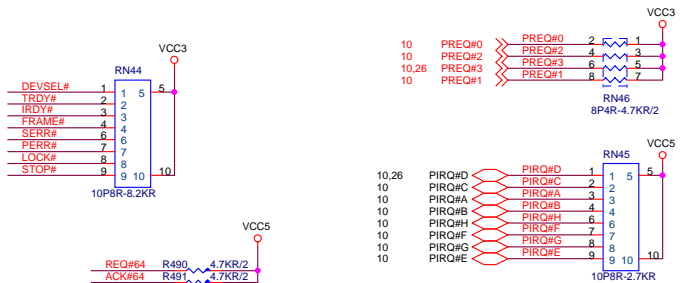
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

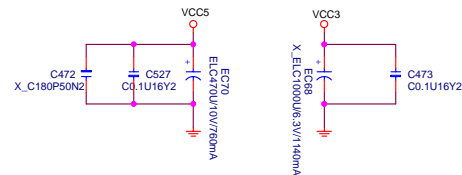


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

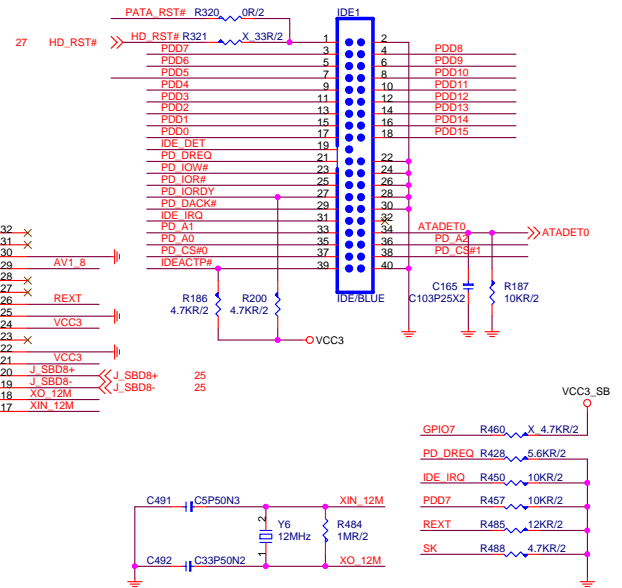
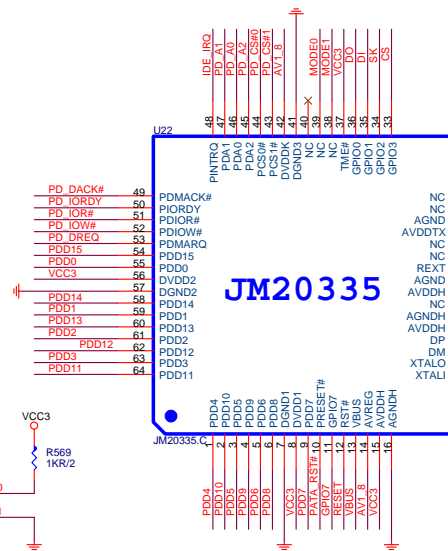
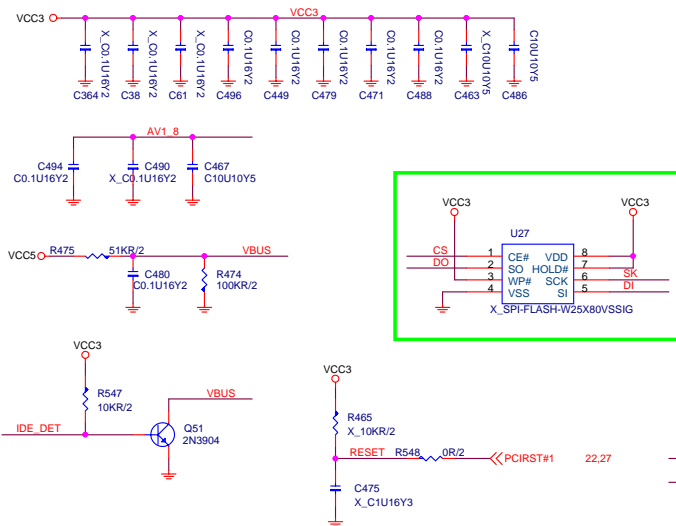


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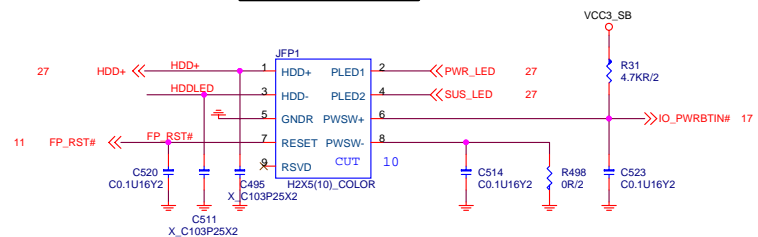
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Size	Document Description	Rev
Custom	PCI Slot 1 & 2	10
Date:	Monday, July 31, 2006	Sheet 23 of 36

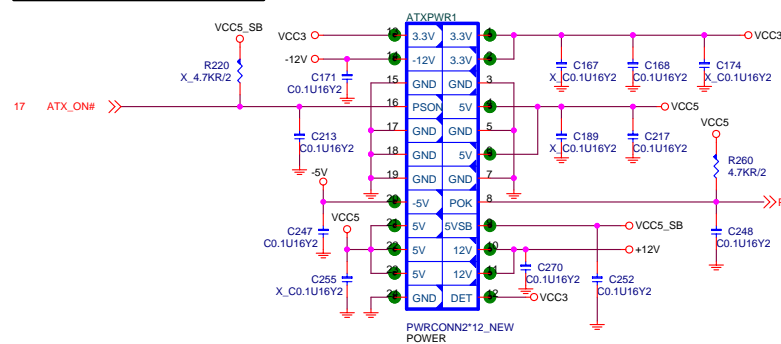
Hi-Speed USB to PATA Bridge



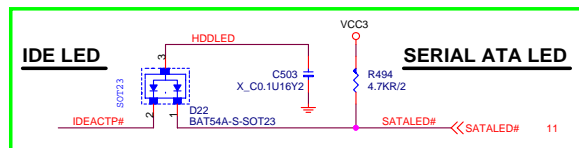
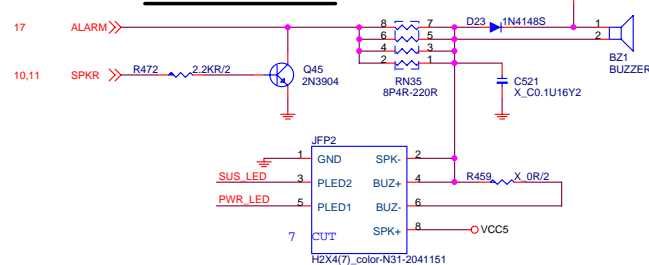
Front Panel



ATX CONNECTOR



BUZZER

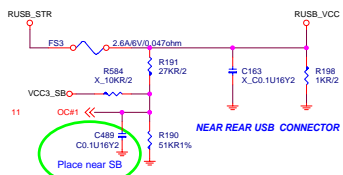


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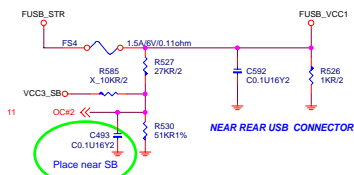
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Size Custom	Document Description ATX, IDE Connector & F_Panel	Rev 10
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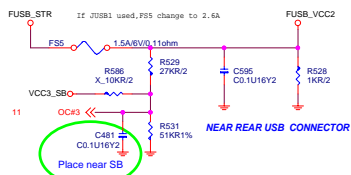
POWER CIRCUIT FOR USB PORT 0,1,2,3



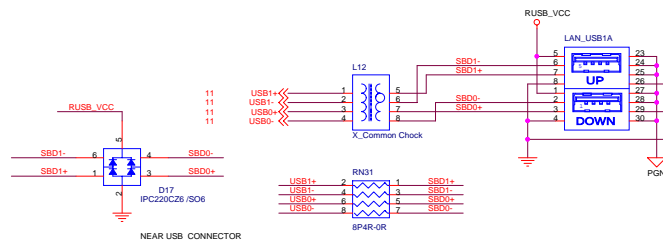
POWER CIRCUIT FOR USB PORT 4,5



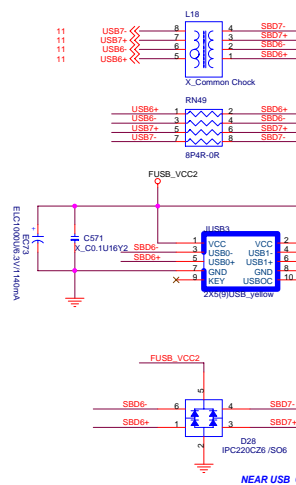
POWER CIRCUIT FOR USB PORT 6,7



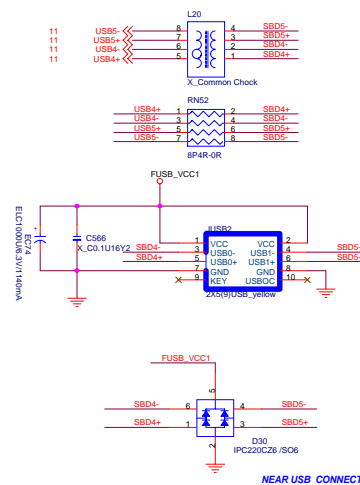
REAR USB CONNECTOR FOR USB PORT 0,1



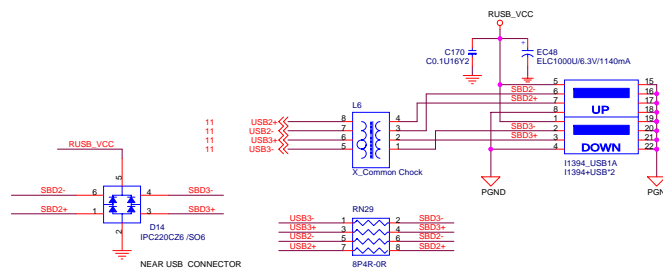
FRONT USB CONNECTOR FOR USB PORT 6,7



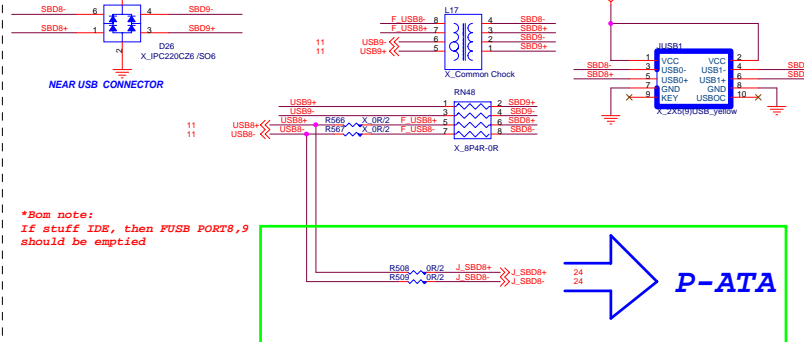
FRONT USB CONNECTOR FOR USB PORT 4,5



REAR USB CONNECTOR FOR USB PORT 2,3



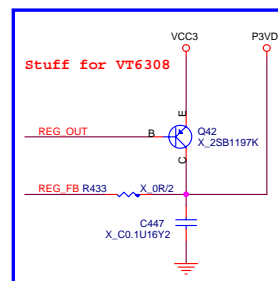
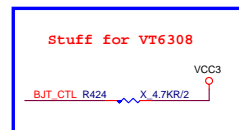
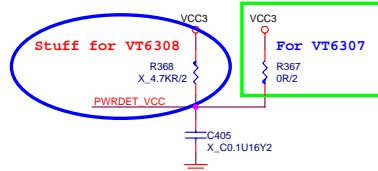
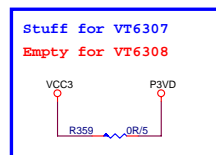
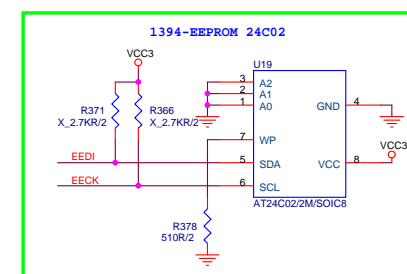
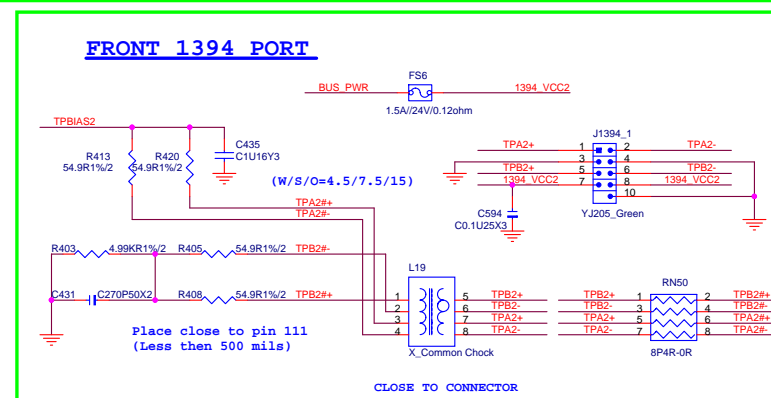
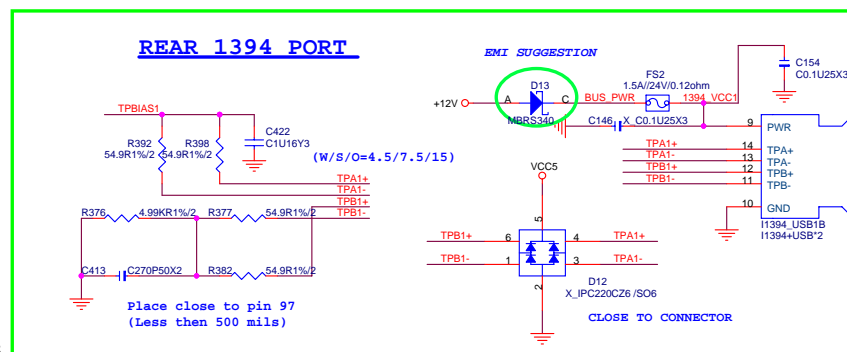
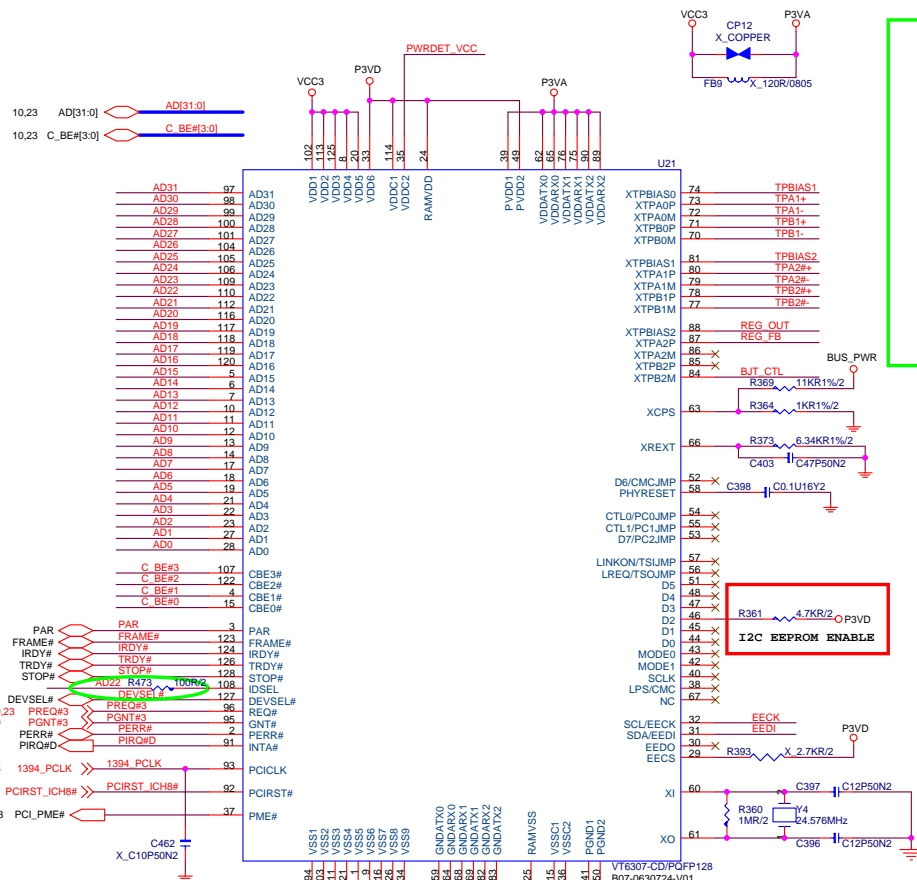
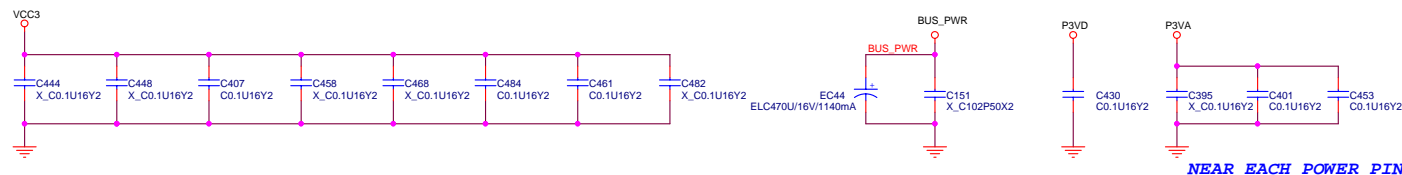
FRONT USB CONNECTOR FOR USB PORT 8,9



*Bom note:
If stuff IDE, then FUSB PORT8,9
should be emptied

Layout時應注意: 將PGND與GND, 在第三層用兩個50mll的通道相連

IEEE-1394



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Custom	IEEE-1394 VT6307 / 6308	

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ACPI Controller MS-7

VDIMM LINEAR OR PWM SELECT

VDIMM MODE EXTRAM
LINEAR REGULATOR PULL LOW
PWM REGULATOR PULL HIGH

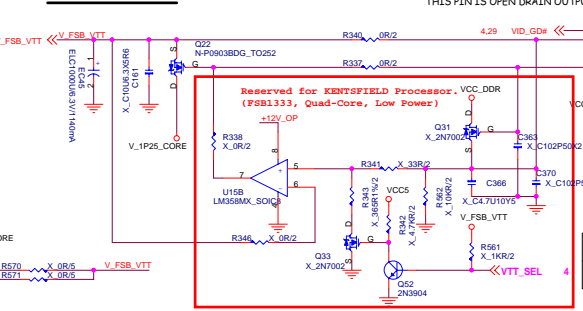
3VSB MODE SELECT

3VSB MODE 3VSDRIVE
SINGLE MOSFET PULL HIGH
DUAL MOSFET PULL LOW

DDR I & DDR II VOLT SELECT

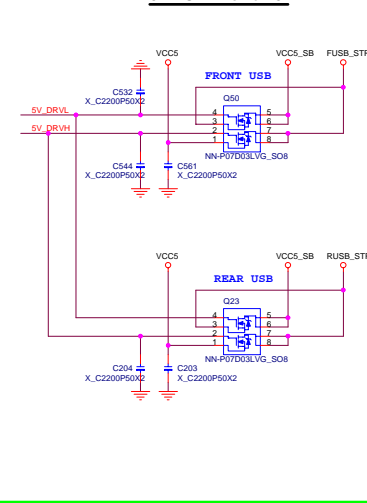
DDR TYPE TOUTHW
PULL LOW 1.5V
PULL HIGH 1.6V

V_FSB_VTT 6.2A

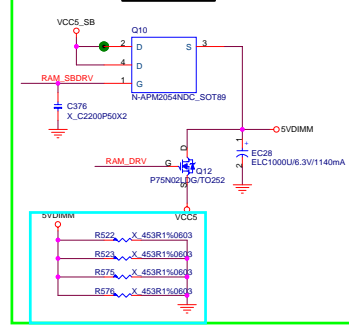


VTT_SEL = H	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core).
VTT_SEL = L	V_FSB_VTT=1.2V	For normal processors.

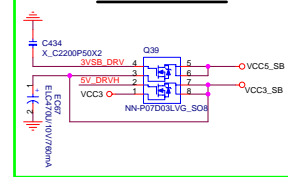
5V DUAL Power 5A



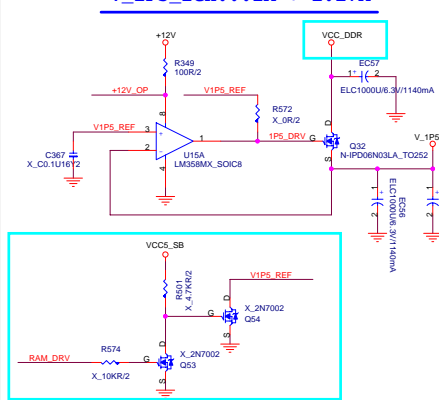
5VDIMM



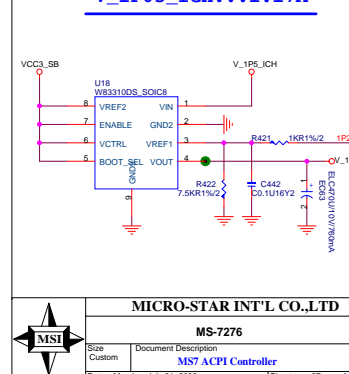
VCC3_SB Power



V_1P5_ICH...2A + 1.17A



V_1P05_ICH...1.17A



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Layout Note:

- 1.Add more and more via at MS11's GND
- 2.All small signal should be referenced to GND

Note: $I_{ripple} = I_{out} \cdot [D/(N \cdot (D \cdot D))] \cdot 0.5 \dots D = V_{out}/V_{in}$

$$I_{ripple} = 25 \cdot 0.48 = 12A$$

$$(2.35 \cdot 2) \cdot 1.7 = 7.99A \approx 12A$$

*Short to V_1P25_CL
if no iAMT support

CHOKE4
CH_12U_18A

CHOKE3
CH_22U_25A

CONNECT TO CHOKE OUTPUT

DCR=1.68mohm

DDR II VTT POWER

DDR II 1.8V POWER...25A

Note: $I_{ripple} = I_{out} * [D/N - (D*D)]^{0.5} \dots D = V_{out}/V_{in}$

$$I_{ripple} = 25 * 0.48 = 12A$$

$$(2.8 + 2.35) * 1.7 = 8.755A < 12A$$

DCR=1.4mohm

Layout Note:

1. Add more and more via at MS11's GND
2. All small signal should be referenced to GND

V_1P25_CL_MCH (3.8A)

For AMT power

S4_STATE#
 AMT Enable-->indication of ACPI S4 state
 SLP_S4#
 AMT Disable-->indicate ACPI S4 state, DRAM power off.
 AMT Enable-->not be asserted ACPI S4 state, DRAM power ON
 AMT Enable SLP_M#-->Control the overall power to Intel
 AMT during ACPI S3-S5.

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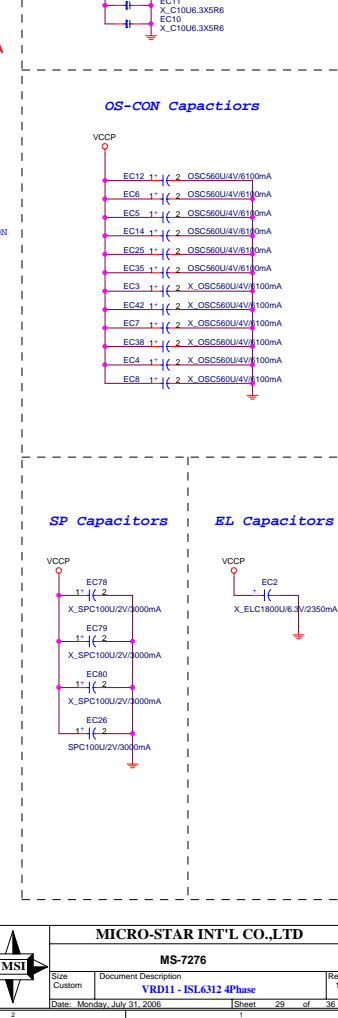
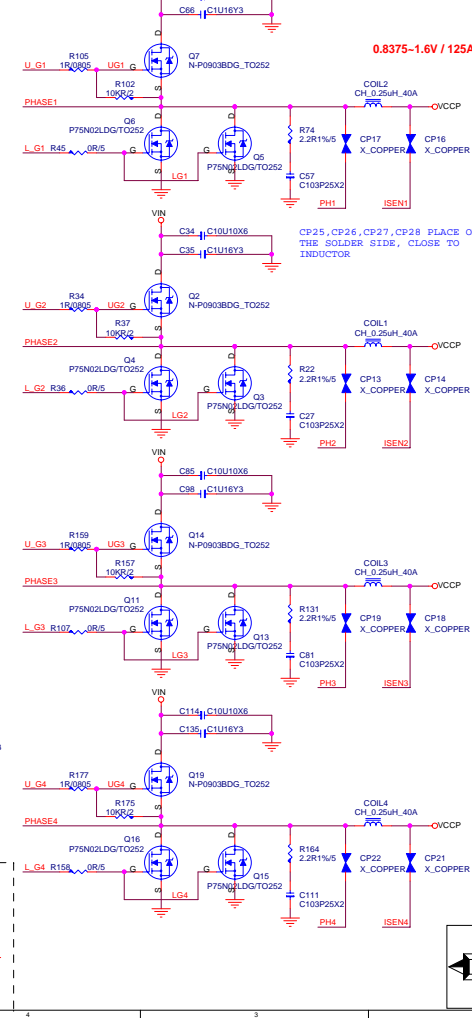
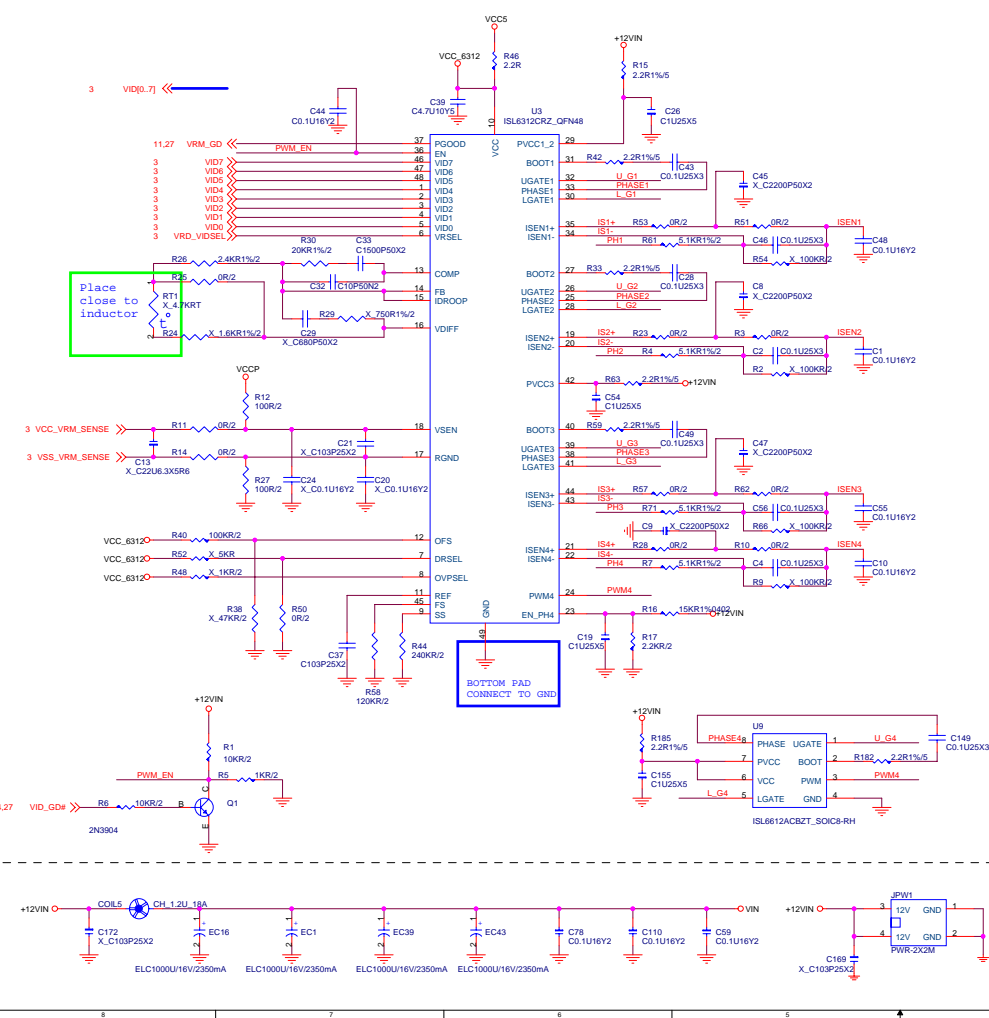
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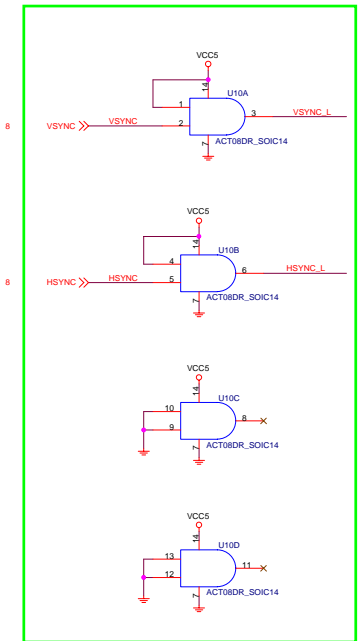
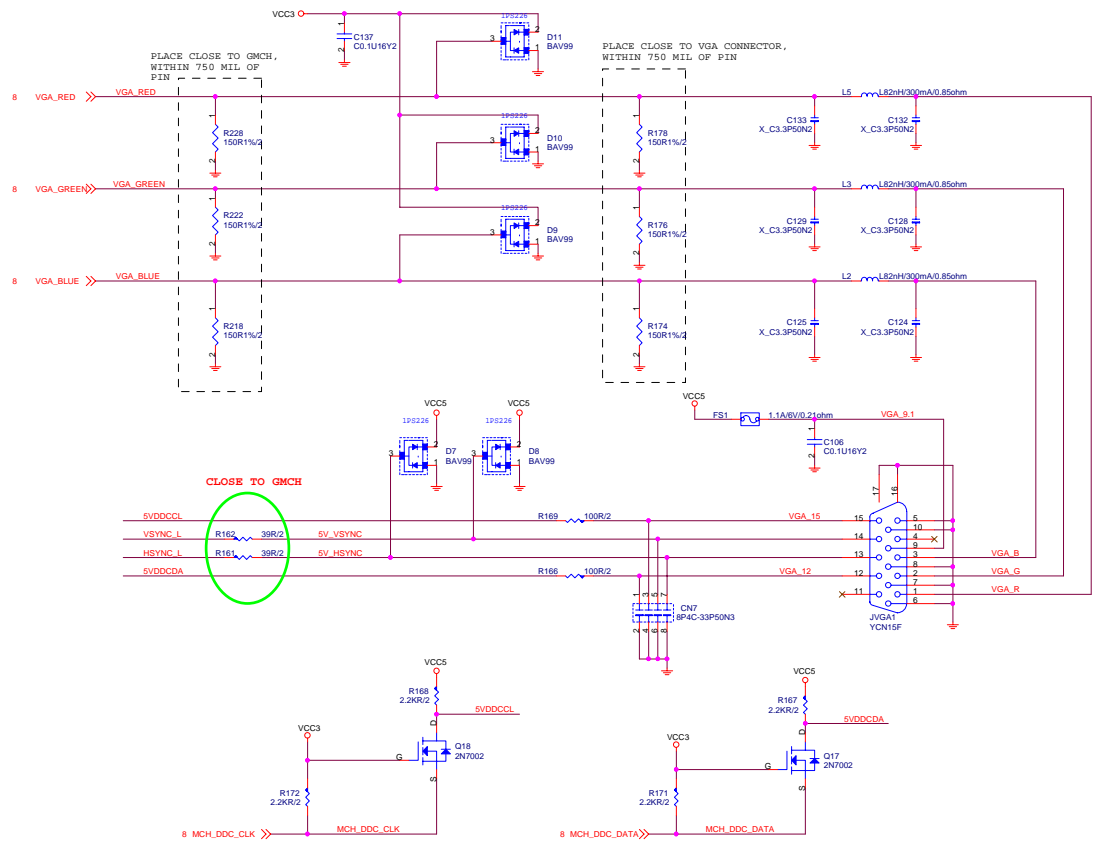
Voltage Regular Module

N-P0903BDG_TO252
P75N02LDG/TO252
C100U25P
CD560U40S-2
1800UF/6.3V
0.25uH/40A
CH-1.1U25A-LF
CD1000U16EL20-2

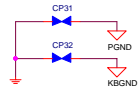
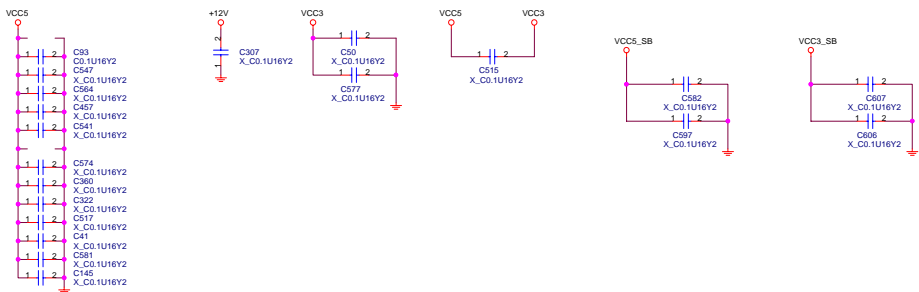
mosfet/n-channel,P0903BDG,SMT/TO252,Rds(on)=9.5m (10V/25A),Vgs(on)=1-3V,Id=50A,Ciss=1800pf,Qg=50nC,Vds=25V,Vgs= 20V,RoHS COMPLIANCE
mosfet/n-channel,P75N02LDG,SMT/TO252,Rds(on)=7m (@10V,30A),Vgs(on)=1-3V,Id=75A,Ciss=5000pf,Qg=140nC,Vds=25V,Vgs= 20V,RoHS COMPLIANCE
ESR<7m,LC<12uH,105C
CH-1.1U25A-LF,ESR<7mohm,Ripplecur.=6100mA ,Lc. <500uA,SPEC series,RoHS compliance
ESR<12m ,Ripplecur.<2350mA,105C, longlife change from 2000hrs to 3000hrs ,K&J
IND CHOKE,0.25uH,20%,DIP/8.5mm,40A,0.6mOhm,, ,PEW,FERRITE,SQUARE,RoHS COMPLIANCE
IND CHOKE,1.1uH,20%,DIP/9mm,25A,1.4mOhm,5.5T,0.9mmx3,PEW,IRON,,LEAD FREE
CAP,EL,1000u,16V,Dip-8x20/3.5mm,20%,12mOhm,2350mA,105C,3000hrs,RoHS COMPLIANCE



Video Connector



EMI Reserved



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ICH8

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name
GPIO[0]	unmuxed		I/O	Core	Y	Y	3.3V	GPI	SIO_SMI#
GPIO[1]	TACH1		I/O	Core	Y	Y	3.3V	GPI	SFAN_TACH
GPIO[5:2]	PIRQ[H:E]#		I/OD	Core	Y	Y	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]		I/O	Core	Y	Y	3.3V	GPI	GPIO_[7:6]
GPIO[8]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	SIO_PME#
GPIO[9]	WOL_EN		I/O	Resume	Y	Y	3.3V	Native	GPIO_9
GPIO[10]	CLGPIO1		I/O	Resume	Y	Y	3.3V	GPI	GPIO_10
GPIO[11]	SMBALERT#		I/O	Resume	Y	Y	3.3V	Native	SMB_ALERT#
GPIO[12]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	ATADET0
GPIO[13]	unmuxed		I/O	Resume	Y	Y	3.3V	GPI	CLEAR_CMOS#
GPIO[14]	CLGPIO2		I/O	Resume	Y	Y	3.3V	GPI	GPIO_14
GPIO[15]	unmuxed		I/O	Resume			3.3V	GPO	
GPIO[16]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[17]	TACH0		I/O	Core	Y		3.3V	GPI	CFAN_TACH
GPIO[18]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[19]	SATA1GP		I/O	Core	Y		3.3V	GPI	GPIO_19
GPIO[20]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[21]	SATA0GP		I/O	Core	Y		3.3V	GPI	GPIO_21
GPIO[22]	SCLOCK		I/O	Core	Y		3.3V	GPI	GPIO_22
GPIO[23]	LDRQ1#		I/O	Core	Y		3.3V	Native	LDRQ_1#
GPIO[24]	CLGPIO0		I/O	Resume			3.3V	GPO	
GPIO[25]	unmuxed		I/O	Resume			3.3V	Native	FRONT_IO#
GPIO[26]	S4_STATE#		I/O	Resume			3.3V	GPO	
GPIO[27]	EL_STATE0		I/O	Resume			3.3V	GPO	
GPIO[28]	EL_STATE1		I/O	Resume			3.3V	GPO	
GPIO[29]	OC5#		I/O	Resume	Y		3.3V	Native	OC#2
GPIO[30]	OC6#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[31]	OC7#		I/O	Resume	Y		3.3V	Native	OC#3
GPIO[32]	unmuxed		I/O	Core			3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed		I/O	Core			3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed		I/O	Core			3.3V	GPO	
GPIO[35]	SATACLKREQ#		I/O	Core			3.3V	GPO	
GPIO[36]	SATA2GP		I/O	Core	Y		3.3V	GPI	GPIO_36
GPIO[37]	SATA3GP		I/O	Core	Y		3.3V	GPI	GPIO_37
GPIO[38]	SLOAD		I/O	Core	Y		3.3V	GPI	GPIO_38
GPIO[39]	SDATAOUT0		I/O	Core	Y		3.3V	GPI	GPIO_39
GPIO[43:40]	OC[4:1]#		I/O	Resume	Y		3.3V	Native	OC#1;OC#2
GPIO[47:44]	NA		NA	NA			NA	NA	Not implemented
GPIO[48]	SDATAOUT1		I/O	Core	Y		3.3V	GPI	GPIO_48
GPIO[49]	CPUPWRGD		I/O	V_CPU_IO			CPU	Native	H_PWRGD
GPIO[50]	REQ1#		I/O	Core	Y		5.5V	Native	PREQ#1
GPIO[51]	GNT1#		I/O	Core			3.3V	Native	PGNT#1
GPIO[52]	REQ2#		I/O	Core	Y		5.5V	Native	PREQ#2
GPIO[53]	GNT2#		I/O	Core			3.3V	Native	PGNT#2
GPIO[54]	REQ3#		I/O	Core	Y		5.5V	Native	PREQ#3
GPIO[55]	GNT3#		I/O	Core			3.3V	Native	PGNT#3

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD20	PCI_CLK1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD21	PCI_CLK2
1394	PIRQ#D	PREQ#3 PGNT#3	AD22	1394_PCLK

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI_E X16 & PCI_E X1
PCIRST#2	SIO, 1394, FWH, TPM
PCIRST#3	PCI SLOT1&2,
PCIRST_ICH8#	MS7
HD_RST#	Primary IDE

DDRII DIMM Config.


DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A1H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A2H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A3H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

JUMPER SETTING

JBAT1	(1-2) NORMAL	(2-3) CLEAR
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0A modify 10 change list

- 1. Add R536 for SLP_M
- 2. Q30.C connect to U8.10
- 3. change VTT_DDR driven from VCC_DDR
- 4. modify ALC883 circuit to meet the Vista "premium" SPEC
- 5. 1394 circuit modify, change net name from "VDD" to "P3VD" (page 26)
- 4. modify ALC883 circuit to meet the Vista "premium" SPEC
- 5. modify JM20335 circuit (page 24)
- 6. modify SMBLINK and SMBCLK/DATA circuit (page 11)
- 7. add C469 C539 for margin (page 12)
- 8. add R564 and R563 for ICS (page 16)
- 9. CPU FAN mornitor from AUXFANOUT change to CPUFANOUT1 (page 17)
- 10. add R566 and R567 for JM20335 (page 25)
- 11. modify V_FSB_VTT circuit (page 27)
- 12. change R51 R3 R62 R10 to 0ohm for power team solution (page 29)
- 13. modify V_1P5_ICH circuit from Vcc3 change to VCC_DDR (page 27)
- 14. Add Q54 and Q53 for S3 sequence (page 27)
- 15. reserve R522 R523 R575 R576 預防逆向電流 (page 27)
- 16. add R578 R579 R580 R581 R582 R583 for 48M and 14M pull high and pull down (page 16)
- 17. Add C606 C607 for EMI (page 30)
- 18. Add R584 R585 R586 for option USB OC# function (page 25)
- 19. change C369 and C371 footprint to 0805 (page 20)
- 20. change 1394`s PCIREST to PCIREST_ICH8 (page 26)

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		MS-7276			
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